TABLE 8-4 Tabular List of Numerical Example

| Addressing | Effective | Content of AC |
|--------------------------------|------------------------------|------------------|
| Direct address | 500 | 800 |
| Immediate operand | 201 | 500 |
| Indirect address | 800 | 300 |
| Relative address | 702 | 325 |
| Indexed address | 600 | 900 |
| | and the second second second | 400 |
| Register indirect | 400 | 700 |
| | 400 | 700 |
| Autoincrement Autodecrement | 399 | 450 |

8-6 Data Transfer and Manipulation

Computers provide an extensive set of instructions to give the user the flexibility to carry out various computational tasks. The instruction set of different computers differ from each other mostly in the way the operands are determined from the address and mode fields. The actual operations available in the instruction set are not very different from one computer to another. It is happens that the binary code assignments in the operation code field is different in different computers, even for the same operation. It may also happen that the symbolic name given to instructions in the assembly language notation is different in different computers, even for the same instruction. Nevertheless there is a set of basic operations that most, if not all, computers include in the instruction repertoire. The basic set of operations available in a typical computer is the subject covered in this and the next section.

Most computer instructions can be classified into three categories:

- 1. Data transfer instructions
 - 2. Data manipulation instructions
 - 3. Program control instructions

Data transfer instructions cause transfer of data from one location to anothe without changing the binary information content. Data manipulation instructions are those that perform arithmetic, logic, and shift operations. Program control instructions provide decision-making capabilities and change the pattaken by the program when executed in the computer. The instruction set a particular computer determines the register transfer operations and control decisions that are available to the user.

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Data Transfer Instructions

Data transfer instructions move data from one place in the computer to another without changing the data content. The most common transfers are between memory and processor registers, between processor registers and input or output, and between the processor registers themselves. Table 8-5 gives a list of eight data transfer instructions used in many computers. Accompanying each instruction is a mnemonic symbol. It must be realized that different computers use different mnemonics for the same instruction name.

The load instruction has been used mostly to designate a transfer from memory to a processor register, usually an accumulator. The store instruction designates a transfer from a processor register into memory. The move instruction has been used in computers with multiple CPU registers to designate a transfer from one register to another. It has also been used for data transfers between CPU registers and memory or between two memory words. The exchange instruction swaps information between two registers or a register and a memory word. The input and output instructions transfer data among processor registers and input or output terminals. The push and pop instructions transfer data between processor registers and a memory stack.

It must be realized that the instructions listed in Table 8-5, as well as in subsequent tables in this section, are often associated with a variety of addressing modes. Some assembly language conventions modify the mnemonic symbol to differentiate between the different addressing modes. For example, the mnemonic for *load immediate* becomes LDI. Other assembly language conventions use a special character to designate the addressing mode. For example, the immediate mode is recognized from a pound sign # placed before the operand. In any case, the important thing is to realize that each instruction can occur with a variety of addressing modes. As an example, consider the *load to accumulator* instruction when used with eight different addressing modes.

TABLE 8-5 Typical Data Transfer
Instructions

| | The second secon | |
|-----------------------|--|----------|
| un operations on data | Name | Mnemonic |
| reputer. The data | 000 | LD |
| ofni beolvib vil | Store | ST |
| | Move | MOV |
| | Exchange | XCH |
| instructions | to the second se | d ball |
| | | OUT |
| | Push | PUSH |
| ions will look y | _ | POP |

entertriction, when executed in the computer must go furnes in

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de 8-3, as well as in

-earle to of address.

-myr pinomenini vil

-nonguage distrem-

placed being the

ach instruction can

consider the load to

addressing models

mode. For example

TABLE 8-6 Eight Addressing Modes for the Load Instruction

| reducing the month of the computer to another dent. The month of the computer to another dent. The month community are between the total and the month of the month of the month of the computers and the month of th | Assembly Convention | Register Transfer |
|--|--|---|
| Direct address Indirect address Relative address Immediate operand Index addressing Register Register indirect | LD ADR LD @ADR LD \$ADR LD #NBR LD ADR(X) LD R1 LD (R1) LD (R1)+ | $AC \leftarrow M[ADR]$ $AC \leftarrow M[M[ADR]]$ $AC \leftarrow M[PC + ADR]$ $AC \leftarrow NBR$ $AC \leftarrow NBR$ $AC \leftarrow M[ADR + XR]$ $AC \leftarrow M[R1]$ $AC \leftarrow M[R1]$ $AC \leftarrow M[R1]$, $R1 \leftarrow R1 +$ |

between CPU registers and memory or between two memory words. The Table 8-6 shows the recommended assembly language convention and the actual transfer accomplished in each case. ADR stands for an address, NBR a number or operand, X is an index register, R1 is a processor register, and A is the accumulator register. The @ character symbolizes an indirect addres The \$ character before an address makes the address relative to the progra counter PC. The # character precedes the operand in an immediate-mod instruction. An indexed mode instruction is recognized by a register that placed in parentheses after the symbolic address. The register mode is symbolic ies, For example, the ized by giving the name of a processor register. In the register indirect mod the name of the register that holds the memory address is enclosed in pare theses. The autoincrement mode is distinguished from the register indire mode by placing a plus after the parenthesized register. The autodecreme mode would use a minus instead. To be able to write assembly langua programs for a computer, it is necessary to know the type of instruction available and also to be familiar with the addressing modes used in the part ular computer. TABLE 8-5 Typical Data Transier

Data Manipulation Instructions

Data manipulation instructions perform operations on data and provide t computational capabilities for the computer. The data manipulation instr tions in a typical computer are usually divided into three basic types:

- 1. Arithmetic instructions
- 2. Logical and bit manipulation instructions
- 3. Shift instructions

A list of data manipulation instructions will look very much like the list microoperations given in Chap. 4. It must be realized, however, that elementary that elementar instruction when executed in the computer must go through the fetch ph to read its binary code value from memory. The operands must also be brought into processor registers according to the rules of the instruction addressing mode. The last step is to execute the instruction in the processor. This last step is implemented by means of microoperations as explained in Chap. 4 or through an ALU and shifter as shown in Fig. 8-2. Some of the arithmetic instructions need special circuits for their implementation.

Arithmetic Instructions The four basic arithmetic operations are addition, subtraction, multiplication, and division. Most computers provide instructions for all four operations. Some small computers have only addition and possibly subtraction instructions. The multiplication and division must then be generated by means of software subroutines. The four basic arithmetic operations are sufficient for formulating solutions to scientific problems when expressed in terms of numerical analysis methods.

A list of typical arithmetic instructions is given in Table 8-7. The increment instruction adds 1 to the value stored in a register or memory word. One common characteristic of the increment operations when executed in processor registers is that a binary number of all 1's when incremented produces a result of all 0's. The decrement instruction subtracts 1 from a value stored in a register or memory word. A number with all 0's, when decremented, produces a number with all 1's.

The add, subtract, multiply, and divide instructions may be available for different types of data. The data type assumed to be in processor registers during the execution of these arithmetic operations is included in the definition of the operation code. An arithmetic instruction may specify fixed-point or floating-point data, binary or decimal data, single-precision or double-preci sion data. The various data types are presented in Chap. 3.

It is not uncommon to find computers with three or more add instruc-

TABLE 8-7 Typical Arithmetic Instructions

| wither Fs complement by medical | Name | Mnemonic | |
|-------------------------------------|--|----------|----------------------|
| dual buts of the appearance. Alther | Particular Contraction of | INC | |
| | Increment | DEC | |
| sed in compation instructions, for | A STATE OF THE PARTY OF THE PAR | ADD | |
| Periorum bit manipulation of | Add | SUB | |
| the body a spirit and 21 the state | Subtract | MUL | |
| an be complemented the | Multiply | DIV | chart se herred bits |
| | Divide | ADDC | |
| deti a bit or liderted graff | Add with carry | SUBB | |
| | Subtract with borrow Negate (2's complement) | NEG | |

tions: one for binary integers, one for floating-point operands, and one for decimal operands. The mnemonics for three add instructions that specify different data types are shown below.

Add two binary integer numbers ADDI Add two floating-point numbers ADDF Add two decimal numbers in BCD ADDD

Algorithms for integer, floating-point, and decimal arithmetic operations

developed in Chap. 10.

developed in Chap. 10.

The number of bits in any register is of finite length and therefore the results of arithmetic operations are of finite precision. Some computers provide hardware double-precision operations where the length of each operand is ambigaction instruct taken to be the length of two memory words. Most small computers provide to employ ve bedaring special instructions to facilitate double-precision arithmetic. A special carry flip-flop is used to store the carry from an operation. The instruction "add with -un to some mi baces carry" performs the addition on two operands plus the value of the carry from the previous computation. Similarly, the "subtract with borrow" instruction subtracts two words and a borrow which may have resulted from a previous subtract operation. The negate instruction forms the 2's complement of number, effectively reversing the sign of an integer when represented in the signed-2's complement form. a season rate in principal averdance with all-0's, when deprended, produces a

Logical and Bit Manipulation Instructions

Logical instructions perform binary operations on strings of bits stored in registers. They are useful for manipulating individual bits or a group of bits that represent binary-coded information. The logical instructions consider each bit of the operand separately and treat it as a Boolean variable. By proper application of the logical instructions it is possible to change bit values, to clear a group of bits, or to insert new bit values into operands stored in registers of memory words.

Some typical logical and bit manipulation instructions are listed in Table 8-8. The clear instruction causes the specified operand to be replaced by 08 The complement instruction produces the 1's complement by inverting all the bits of the operand. The AND, OR, and XOR instructions produce the conte sponding logical operations on individual bits of the operands. Although the perform Boolean operations, when used in computer instructions, the logical There are three by There are three bit manipulation operations possible: a selected bit can be cleared to 0. cleared to 0, or can be set to 1, or can be complemented. The three logical instructions are used. instructions are usually applied to do just that.

The AND instruction is used to clear a bit or a selected group of bits an operand. For any Boolean variable x, the relationships x b0 = 0 and xb1 dictate that a binary variable x. dictate that a binary variable ANDed with a 0 produces a 0; but the variable $\frac{1}{2}$

clear selected bits

may be available for

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on or double-preci

or inner add instruc-

TABLE 8-8 Typical Logical and Bit Manipulation Instructions

| Name | Mnemonic |
|--------------------------------------|--|
| Clear Complement AND OR Exclusive-OP | CLR COM AND OR XOR CLRC SETC |

does not change in value when ANDed with a 1. Therefore, the AND instruction can be used to clear bits of an operand selectively by ANDing the operand with another operand that has 0's in the bit positions that must be cleared. The AND instruction is also called a mask because it masks or inserts 0's in a selected portion of an operand.

exelected bits

The OR instruction is used to set a bit or a selected group of bits of an operand. For any Boolean variable x, the relationships x + 1 = 1 and x + 0 = xdictate that a binary variable ORed with a 1 produces a 1; but the variable does not change when ORed with a 0. Therefore, the OR instruction can be used to selectively set bits of an operand by ORing it with another operand with 1's in the bit positions that must be set to 1.

plement selected

Similarly, the XOR instruction is used to selectively complement bits of an operand. This is because of the Boolean relationships $x \oplus 1 = x'$ and $x \oplus 0 = x$. Thus a binary variable is complemented when XORed with a 1 but does not change in value when XORed with a 0. Numerical examples showing the three logic operations are given in Sec. 4-5.

A few other bit manipulation instructions are included in Table 8-8. Individual bits such as a carry can be cleared, set, or complemented with appropriate instructions. Another example is a flip-flop that controls the interrupt facility and is either enabled or disabled by means of bit manipulation instructions.

Shift Instructions

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Instructions to shift the content of an operand are quite useful and are often provided in several variations. Shifts are operations in which the bits of a word are moved to the left or right. The bit shifted in at the end of the word determines the type of shift used. Shift instructions may specify either logical Kerate ich through carry

be 4 VD insure-

x = 0 - x bras i = i

but the variable does

struction can be used

complement bits of

bris 'x = 1 (1) r equit

and I a dilw took OX a

ed examples showing

shifts, arithmetic shifts, or rotate-type operations. In either case the shift may

be to the right or to the left.

the right or to the left.

Table 8-9 lists four types of shift instructions. The logical shift inserts

Table 8-9 lists four types of shift instructions the leftmost bit for shift right. Table 8-9 lists four types of still the leftmost bit for shift right to the end bit position. The end position is the leftmost bit for shift right and to the end bit position. The end position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually to the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. Arithmetic shifts usually the rightmost bit position for the shift left. the rightmost bit position for the singlement numbers. These rules are given form with the rules for signed-2's complement numbers. These rules are given form with the rules for signed-2 storing form with the rules for signed-2 storing form with the rules for signed-2 storing form with the given in Sec. 4-6. The arithmetic shift-right instruction must preserve the sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign bit is shifted to the right together with the rules for sign between the rules for sign be in Sec. 4-6. The arithmetic similaring the sign bit is shifted to the right together with the the leftmost position. The sign bit itself remains unchanged. This is a shift the left to the rest together with the leftmost position. The sign bit itself remains unchanged. This is a shift-right of the number, but the sign bit itself remains unchanged. The arithmetic shift is of the number, but the sign bit remaining the same. The arithmetic shift-left in operation with the end bit remaining the same. The arithmetic shift-left in operation with the end bit remains and is identical to the logical shift-less struction inserts 0 to the end position and is identical to the logical shift-less struction inserts 0 to the end possession struction inserts of the left instruction. For this reason many computers do not provide a distinct anthe instruction is instruction. For this reason much struction is already metic shift-left instruction when the logical shift-left instruction is already available.

The rotate instructions produce a circular shift. Bits shifted out at one end of the word are not lost as in a logical shift but are circulated back into the other end. The rotate through carry instruction treats a carry bit as an extension the register whose word is being rotated. Thus a rotate-left through cam instruction transfers the carry bit into the rightmost bit position of the register transfers the leftmost bit position into the carry, and at the same time, shift the entire register to the left.

Some computers have a multiple-field format for the shift instructions cred woup or bits of an One field contains the operation code and the others specify the type of shi and the number of times that an operand is to be shifted. A possible instruction code format of a shift instruction may include five fields as follows: with appoint operand with I's

OP REG TYPE RL COUNT

Here OP is the operation code field; REG is a register address that specifies the location of the operand; TYPE is a 2-bit field specifying the four different type of shifts; RL is a 1-bit field specifying a shift right or left; and COUNT is akfield specifying up to $2^k - 1$ shifts. With such a format, it is possible to specified the type of shift, the direction, and the number of shifts, all in one instruction

such as a carry can be cleared, set, or complemented with TABLE 8-9 Typical Shift Instructions and is either enabled or disabled by means of bit manipulation

8-7 Program Control

Instructions are always stored in successive memory locations. When processed in the CPU, the instructions are fetched from consecutive memory locations and executed. Each time an instruction is fetched from memory, the program counter is incremented so that it contains the address of the next instruction in sequence. After the execution of a data transfer or data manipulation instruction, control returns to the fetch cycle with the program counter containing the address of the instruction next in sequence. On the other hand, a program control type of instruction, when executed, may change the address value in the program counter and cause the flow of control to be altered. In other words, program control instructions specify conditions for altering the content of the program counter, while data transfer and manipulation instructions specify conditions for data-processing operations. The change in value of the program counter as a result of the execution of a program control instruction causes a break in the sequence of instruction execution. This is an important feature in digital computers, as it provides control over the flow of program execution and a capability for branching to different program segments.

Some typical program control instructions are listed in Table 8-10. The branch and jump instructions are used interchangeably to mean the same thing, but sometimes they are used to denote different addressing modes. The branch is usually a one-address instruction. It is written in assembly language as BR ADR, where ADR is a symbolic name for an address. When executed, the branch instruction causes a transfer of the value of ADR into the program counter. Since the program counter contains the address of the instruction to be executed, the next instruction will come from location ADR.

Branch and jump instructions may be conditional or unconditional. An unconditional branch instruction causes a branch to the specified address without any conditions. The conditional branch instruction specifies a condition such as branch if positive or branch if zero. If the condition is met, the program counter is loaded with the branch address and the next instruction is taken

TABLE 8-10 Typical Program Control Instructions

| inest-order bit. It is seller | Name | Mnemonic |
|-------------------------------------|---|----------|
| the state of the order and one | there is the second (many) | BR |
| at of the ALU contains all its life | Branch (0195) | JMP |
| AND SHEETINGS OF THE SERVICE | | SKP |
| and a true output is a Single | Skip | CALL |
| | Call | - CT |
| exclusive-OR or the last the | Return (haraction) | |
| Afterwase, This is the condi- | Compare (by subtraction) Test (by ANDing) | TST |

TABLE 8-11 Conditional Branch Instructions

| | Mnemonic | Branch condition | Tested condition |
|-------------------------------|-----------------|--------------------------------|-------------------|
| | | Branch if zero | Z=1 |
| | BZ | Branch if not zero | Z=0 |
| | BNZ | | C=1 |
| | BC | Branch if carry | C = 0 |
| | BNC | Branch if no carry | S = 0 |
| | BP | Branch if plus | |
| | BM | Branch II IIIIIus | V=1 |
| | BV | Branch if overflow | |
| | BNV | Branch if no overflow | semiun = 0 with |
| | Unsigned | d compare conditions $(A - B)$ | a program sector |
| | BHI | Branch if higher | A > B |
| | BHE | Branch if higher or equal | $A \geq B$ |
| | BLO | Branch if lower | A < B |
| | BLOE | Branch if lower or equal | $A \leq B$ |
| | BE | Branch if equal | A = B |
| J. Dogingk | BNE | Branch if not equal | 11 7- D |
| birs, a | Signed o | compare conditions $(A - B)$ | retaining the res |
| | BGT | Branch if greater than | A > B |
| 75 E 3 1 1 | DCE | Branch if greater or equal | $A \geq B$ |
| a complement (see Sec. 3-3). | THE PROPERTY OF | Branch if less than | A < B |
| eater than + 117 or less than | BLE | Branch if less or equal | |
| | BE | Branch if equal | $A \leq B$ |
| | BNE | Branch if not equal | A = B |
| ill operation to determine | A DE YOUR FINE | Dianell II Hot equal | $A \neq B$ |

inserted to define the 0 state. Thus BC is Branch on Carry, and BNC is Branch on No Carry. If the stated condition is true, program control is transferred the address specified by the instruction. If not, control continues with the instruction that follows. The conditional instructions can be associated alwith the jump, skip, call, or return type of program control instructions.

The zero status bit is used for testing if the result of an ALU operation is equal to zero or not. The carry bit is used to check if there is a carry out the most significant bit position of the ALU. It is also used in conjunction with un listed in Table 8-10 the rotate instructions to check the bit shifted from the end position of a regist into the carry position. The sign bit reflects the state of the most significant b of the output from the ALU. S = 0 denotes a positive sign and S = 1, a negative sign. Therefore S = 1, a negative S = 1, and S = 1, a negative S = 1, and S = 1sign. Therefore, a branch on plus checks for a sign bit of 0 and a branch of minus checks for a sign bit of 0 and a branch of the checks for a sign between the checks f minus checks for a sign bit of 1. It must be realized, however, that these two ons. Each mount conditional branch instructions can be used to check the value of the mot significant bit and a little of the mot significant ation of the condition significant bit whether it represents a sign or not. The overflow bit is used letter N (for no) is conjunction with arithmetic operations done on signed numbers in 2's complement representation ment representation.