- Design an interfacing circuit to set up the 8255A in the handshake mode (Mode 1) and write instructions to transfer data under status check I/O and interrupt I/O.
- Explain the operating modes of the 8254 timer and write instructions to set up the timer in the various modes.
- Explain the functions of the 8259A interrupt controller and its operation in the fully nested mode.
- Explain the process of the Direct Memory Access (DMA) and the functions of various elements of the 8237.

## 15.1 THE 8255A PROGRAMMABLE PERIPHERAL INTERFACE

The 8255A is a widely used, programmable, parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile, and economical (when multiple I/O ports are required), but somewhat complex. It is an important general-purpose I/O device that can be used with almost any microprocessor.

The 8255A has 24 I/O pins that can be grouped primarily in two 8-bit parallel ports: A and B, with the remaining eight bits as port C. The eight bits of port C can be used as individual bits or be grouped in two 4-bit ports: $C_{UPPER}$ ($C_U$) and $C_{LOWER}$ ($C_L$), as in Figure 15.1(a). The functions of these ports are defined by writing a control word in the control register.

Figure 15.1(b) shows all the functions of the 8255A, classified according to two modes: the Bit Set/Reset (BSR) mode and the I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into three modes: Mode 0, Mode 1, and Mode 2. In Mode 0, all ports function as simple I/O ports. Mode 1 is a handshake mode whereby ports A and/or B use bits from port C as handshake signals. In the handshake mode, two types of I/O data transfer can be implemented: status check and interrupt. In Mode 2, port A can be set up for bidirectional data transfer using handshake signals from port C, and port B can be set up either in Mode 0 or Mode 1.

### 15.1.1 Block Diagram of the 8255A

The block diagram in Figure 15.2(a) shows two 8-bit ports (A and B), two 4-bit ports ($C_U$ and $C_L$), the data bus buffer, and control logic. Figure 15.2(b) shows a simplified but expanded version of the internal structure, including a control register. This block diagram includes all the elements of a programmable device; port C performs functions similar to that of the status register in addition to providing handshake signals.

#### CONTROL LOGIC

The control section has six lines. Their functions and connections are as follows:

- $\overline{RD}$ **(Read):** This control signal enables the Read operation. When the signal is low, the MPU reads data from a selected I/O port of the 8255A.
- $\overline{WR}$ **(Write):** This control signal enables the Write operation. When the signal goes low, the MPU writes into a selected I/O port or the control register.

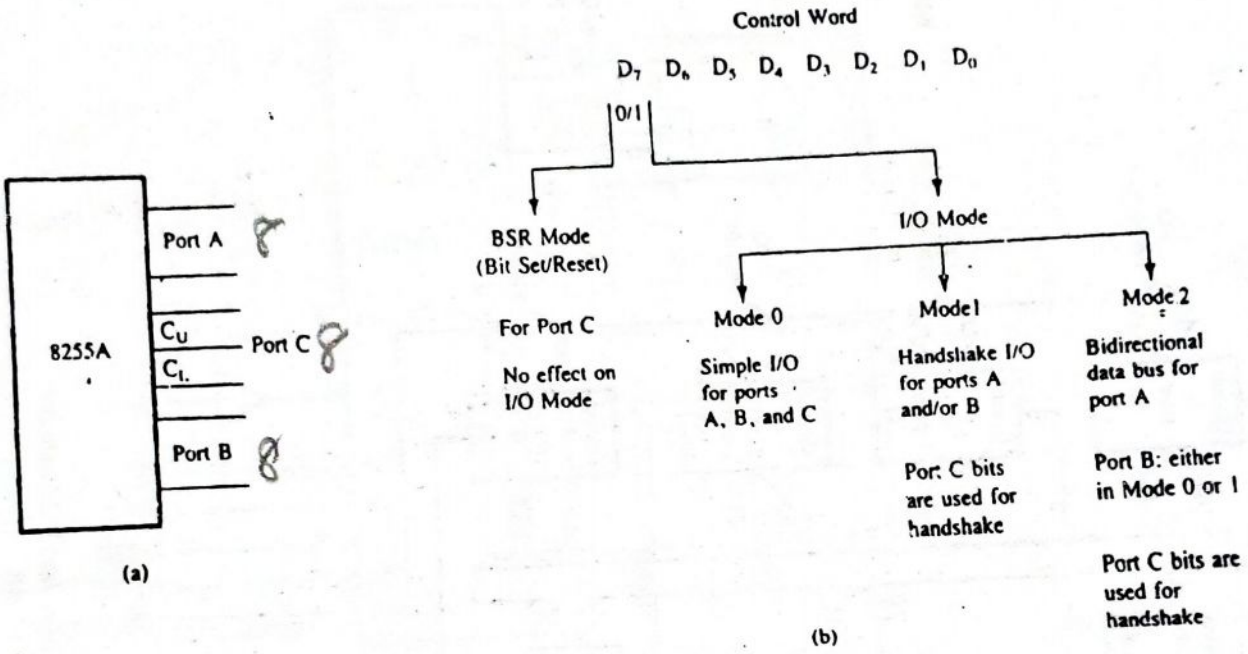


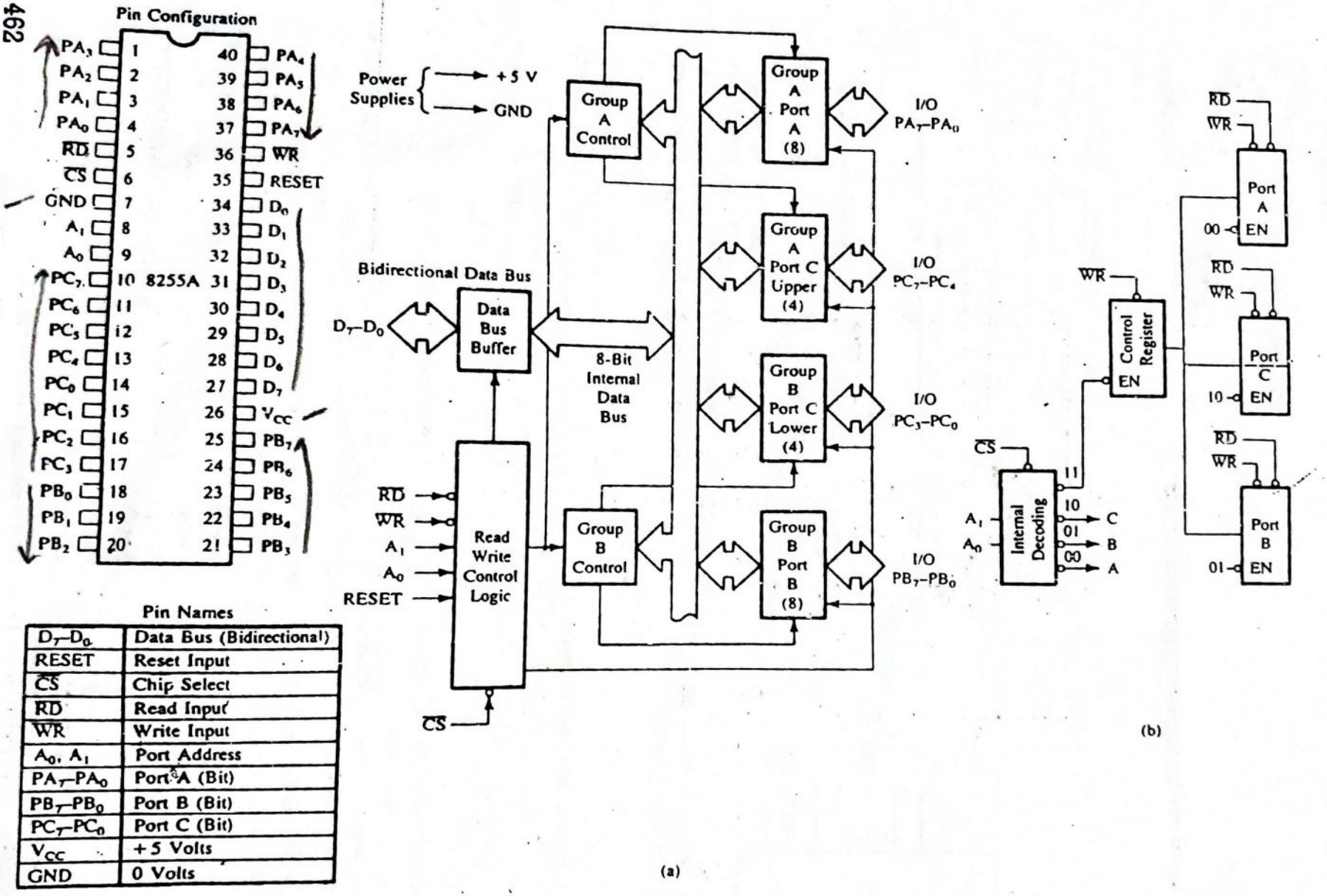

FIGURE 15.1
8255A I/O Ports (a) and Their Modes (b)

- **RESET (Reset):** This is an active high signal; it clears the control register and sets all ports in the input mode.
- **$\overline{CS}$, $A_0$, and $A_1$:** These are device select signals. $\overline{CS}$ is connected to a decoded address, and $A_0$ and $A_1$ are generally connected to MPU address lines $A_0$ and $A_1$, respectively.

The $\overline{CS}$ signal is the master Chip Select, and $A_0$ and $A_1$ specify one of the I/O ports or the control register as given below:

| $\overline{CS}$ | $A_1$ | $A_0$ | Selected |
|---|---|---|---|
| 0 | 0 | 0 | Port A |
| 0 | 0 | 1 | Port B |
| 0 | 1 | 0 | Port C |
| 0 | 1 | 1 | Control Register |
| 1 | X | X | 8255A is not selected. |

As an example, the port addresses in Figure 15.3(a) are determined by the $\overline{CS}$, $A_0$, and $A_1$ lines. The $\overline{CS}$ line goes low when $A_7 = 1$ and $A_6$ through $A_2$ are at logic 0. When these signals are combined with $A_0$ and $A_1$, the port addresses range from 80H to 83H, as shown in Figure 15.3(b).

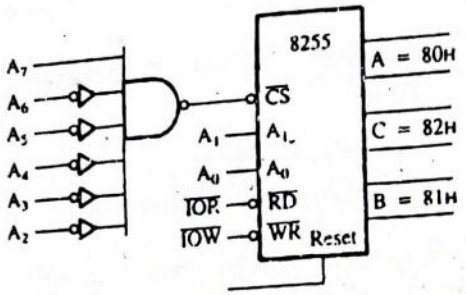



Pin Names

| | |
|---|---|
| $D_7$–$D_0$ | Data Bus (Bidirectional) |
| RESET | Reset Input |
| $\overline{CS}$ | Chip Select |
| $\overline{RD}$ | Read Input |
| $\overline{WR}$ | Write Input |
| $A_0$, $A_1$ | Port Address |
| $PA_7$–$PA_0$ | Port A (Bit) |
| $PB_7$–$PB_0$ | Port B (Bit) |
| $PC_7$–$PC_0$ | Port C (Bit) |
| $V_{CC}$ | +5 Volts |
| GND | 0 Volts |

**FIGURE 15.2**
8255A Block Diagram (a) and an Expanded Version of the Control Logic and I/O Ports (b)

SOURCE: A: Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3-100.




(a)

| $\overline{CS}$ | | Hex Address | Port |
|---|---|---|---|
| $A_7$ $A_6$ $A_5$ $A_4$ $A_3$ $A_2$ | $A_1$ $A_0$ | | |
| 1 0 0 0 0 0 | 0 0 | = 80H | A |
| | 0 1 | = 81H | B |
| | 1 0 | = 82H | C |
| | 1 1 | = 83H | Control Register |

(b)

FIGURE 15.3
8255A Chip Select Logic (a) and I/O Port Addresses (b)

### CONTROL WORD

Figure 15.2(b) shows a register called the **control register.** The contents of this register, called the **control word,** specify an I/O function for each port. This register can be accessed to write a control word when $A_0$ and $A_1$ are at logic 1, as mentioned previously. The register is not accessible for a Read operation.

Bit $D_7$ of the control register specifies either the I/O function or the Bit Set/Reset function, as classified in Figure 15.1(b). If bit $D_7 = 1$, bits $D_6$–$D_0$ determine I/O functions in various modes, as shown in Figure 15.4. If bit $D_7 = 0$, port C operates in the Bit Set/Reset (BSR) mode. The BSR control word does not affect the functions of ports A and B (the BSR mode will be described later).

To communicate with peripherals through the 8255A, three steps are necessary:

1. Determine the addresses of ports A, B, and C and of the control register according to the Chip Select logic and address lines $A_0$ and $A_1$.
2. Write a control word in the control register.
3. Write I/O instructions to communicate with peripherals through ports A, B, and C.

Examples of the various modes are given in the next section.

## 15.1.2 Mode 0: Simple Input or Output

In this mode, ports A and B are used as two simple 8-bit I/O ports and port C as two 4-bit ports. Each port (or half-port, in case of C) can be programmed to function as simply an input port or an output port. The input/output features in Mode 0 are as follows:

1. Outputs are latched.
2. Inputs are not latched.
3. Ports do not have handshake or interrupt capability.

---

**Example 15.1**

1. Identify the port addresses in Figure 15.5.
2. Identify the Mode 0 control word to configure port A and port $C_U$ as output ports and port B and port $C_L$ as input ports.

FIGURE 15.2
8255A Block Diagram (a) and an Expanded Version of the Control Logic and I/O Ports (b)
SOURCE: A: Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3-100.

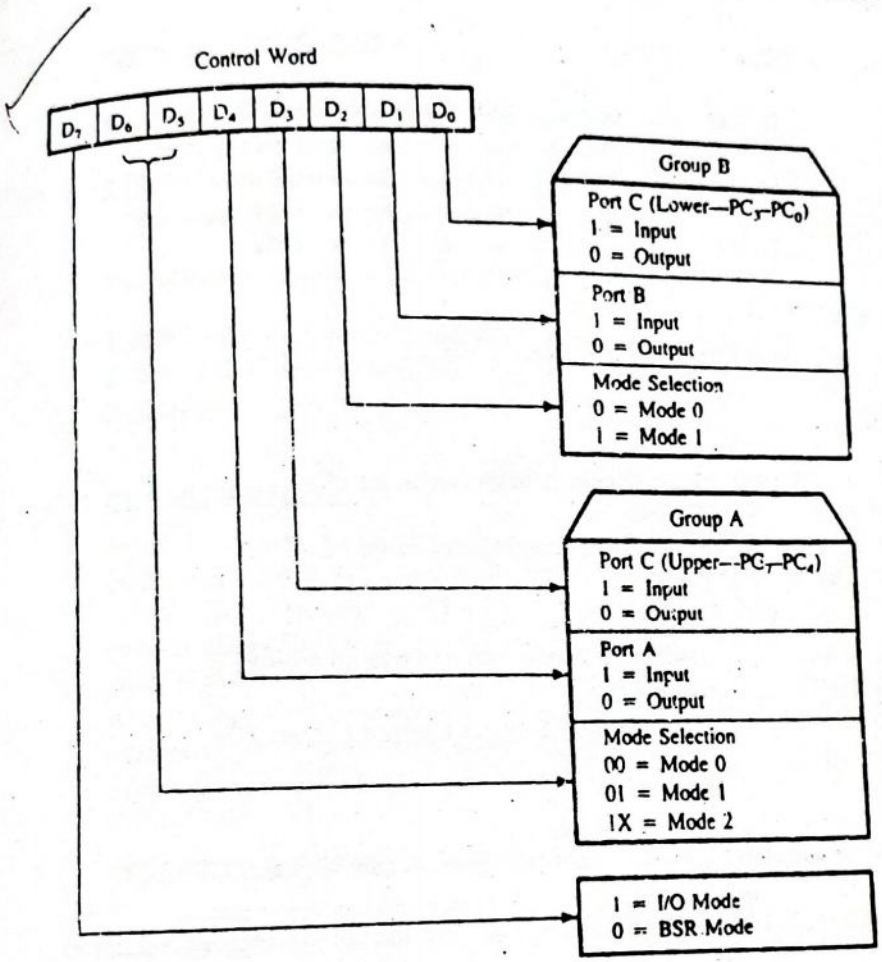



FIGURE 15.4
8255A Control Word Format for I/O Mode

SOURCE: Adapted from Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3-104.

3. Write a program to read the DIP switches and display the reading from port B at port A and from port $C_L$ at port $C_U$.

**1. Port Addresses** This is a memory-mapped I/O; when the address line $A_{15}$ is high, the Chip Select line is enabled. Assuming all don't care lines are at logic 0, the port addresses are as follows:

| | | |
|---|---|---|
| Port A | = | 8000H ($A_1 = 0, A_0 = 0$) |
| Port B | = | 8001H ($A_1 = 0, A_0 = 1$) |
| Port C | = | 8002H ($A_1 = 1, A_0 = 0$) |
| Control Register | = | 8003H ($A_1 = 1, A_0 = 1$) |

```
RLC
RLC
STA 8002H      :Display data at port C_U
HLT
```

**Program Description** The circuit is designed for memory-mapped I/O; therefore, the instructions are written as if all the 8255A ports are memory locations.

The ports are initialized by placing the control word 83H in the control register. The instructions STA and LDA are equivalent to the instructions OUT and IN, respectively.

In this example, the low four bits of port C are configured as input and the high four bits are configured as output; even though port C has one address for both halves $C_U$ and $C_L$ (8002H). Read and Write operations are differentiated by the control signals $\overline{MEMR}$ and $\overline{MEMW}$. When the MPU reads port C (e.g., LDA 8002H), it receives eight bits in the accumulator. However, the high-order bits ($D_7$–$D_4$) must be ignored because the input data bits are in $PC_3$–$PC_0$. To display these bits at the upper half of port C, bits ($PC_3$–$PC_0$) must be shifted to $PC_7$–$PC_4$.

## 15.1.3 BSR (Bit Set/Reset) Mode

The BSR mode is concerned only with the eight bits of port C, which can be set or reset by writing an appropriate control word in the control register. A control word with bit $D_7$ = 0 is recognized as a BSR control word, and it does not alter any previously transmitted control word with bit $D_7$ = 1; thus the I/O operations of ports A and B are not affected by a BSR control word. In the BSR mode, individual bits of port C can be used for applications such as an on/off switch.

### BSR CONTROL WORD

This control word, when written in the control register, sets or resets one bit at a time, as specified in Figure 15.6.

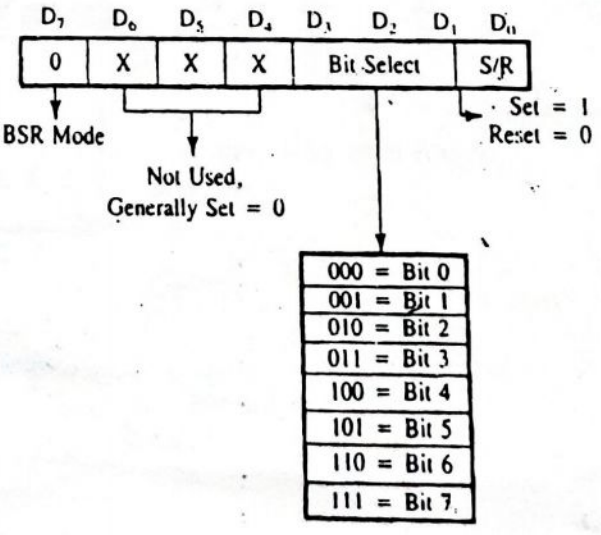



FIGURE 15.6
8255A Control Word Format in the BSR Mode

```
        MVI A, 00001011   ;Word to set PC5 to turn on the fan
        OUT CNTRL         ;Turn on the fan
        POP PSW           ;Retrieve A and flags
        RET
FANOFF: PUSH PSW          ;Save A and flags
        MVI A, 00001010   ;Word to reset PC5 to turn off the fan
        OUT CNTRL         ;Turn off the fan
        POP PSW           ;Retrieve A and flags
        RET
```

HEATON and HEATOFF are subroutines similar to FANON and FANOFF except that they turn on/off the bit $PC_6$.



### PROGRAM DESCRIPTION

The subroutine initializes port A and the lower half of port C as inputs and the upper half of Port C as outputs. It disables $\overline{RD}$ and asserts $\overline{WR}$ signals. When $\overline{WR}$ goes low, the conversion begins and the $\overline{INTR}$ goes high. When the conversion is complete, the $\overline{INTR}$ goes low, indicating that the data byte is ready for reading (see Figure 13.13). The INTR signal can be read as input in a loop or it can be used to interrupt the processor.

The subroutine reads port C and places the status of $PC_0$ in the carry flag by rotating the bit right. If the CY flag is logic 1, the subroutine goes back to the label READ and reads Port C again. The subroutine stays in the loop until $PC_0$ is at logic zero. Once $PC_0$ goes low, the processor asserts $\overline{RD}$ low and reads the data byte. This data byte is already hardware calibrated to be read in degrees Centigrade. The subroutine compares the reading in A with the high set point (35°C). If the comparison does not generate a carry, it means the reading in A is higher than 35°C, and it calls a subroutine FANON to turn on the fan. If it generates a carry, it means the reading in A is lower than 35°C, and it turns off the fan by calling the subroutine FANOFF. However, the subroutine does not check whether a fan is already off or on; in some instances this may be a redundant action. Next it compares the reading with the low set point (10°C). If the reading is lower than 10°C, it calls the subroutine HEATON and if it is higher than 10°C, it calls the subroutine HEATOFF. The subroutines FANON, FANOFF, HEATON, and HEATOFF turn on/off bits $PC_5$ and $PC_6$ connected to the fan and the heater.

## 15.1.5 Mode 1: Input or Output with Handshake

In Mode 1, handshake signals are exchanged between the MPU and peripherals prior to data transfer. The features of this mode include the following:

1. Two ports (A and B) function as 8-bit I/O ports. They can be configured either as input or output ports.
2. Each port uses three lines from port C as handshake signals. The remaining two lines of port C can be used for simple I/O functions.
3. Input and output data are latched.
4. Interrupt logic is supported.

In the 8255A, the specific lines from port C used for handshake signals vary according to the I/O function of a port. Therefore, input and output functions in Mode 1 are discussed separately.

## MODE 1: INPUT CONTROL SIGNALS

Figure 15.8(a) shows the associated control signals used for handshaking when ports A and B are configured as input ports. Port A uses the upper three signals: $PC_3$, $PC_4$, and $PC_5$. Port B uses the lower three signals: $PC_2$, $PC_1$, and $PC_0$. The functions of these signals are as follows:

- $\overline{\text{STB}}$ (Strobe Input): This signal (active low) is generated by a peripheral device to indicate that it has transmitted a byte of data. The 8255A, in response to $\overline{\text{STB}}$, generates IBF and INTR, as shown in Figure 15.9.
- **IBF (Input Buffer Full):** This signal is an acknowledgment by the 8255A to indicate that the input latch has received the data byte. This is reset when the MPU reads the data (Figure 15.9).
- **INTR (Interrupt Request):** This is an output signal that may be used to interrupt the MPU. This signal is generated if $\overline{\text{STB}}$, IBF, and INTE (Internal flip-flop) are all at logic 1. This is reset by the falling edge of the $\overline{\text{RD}}$ signal (Figure 15.9).

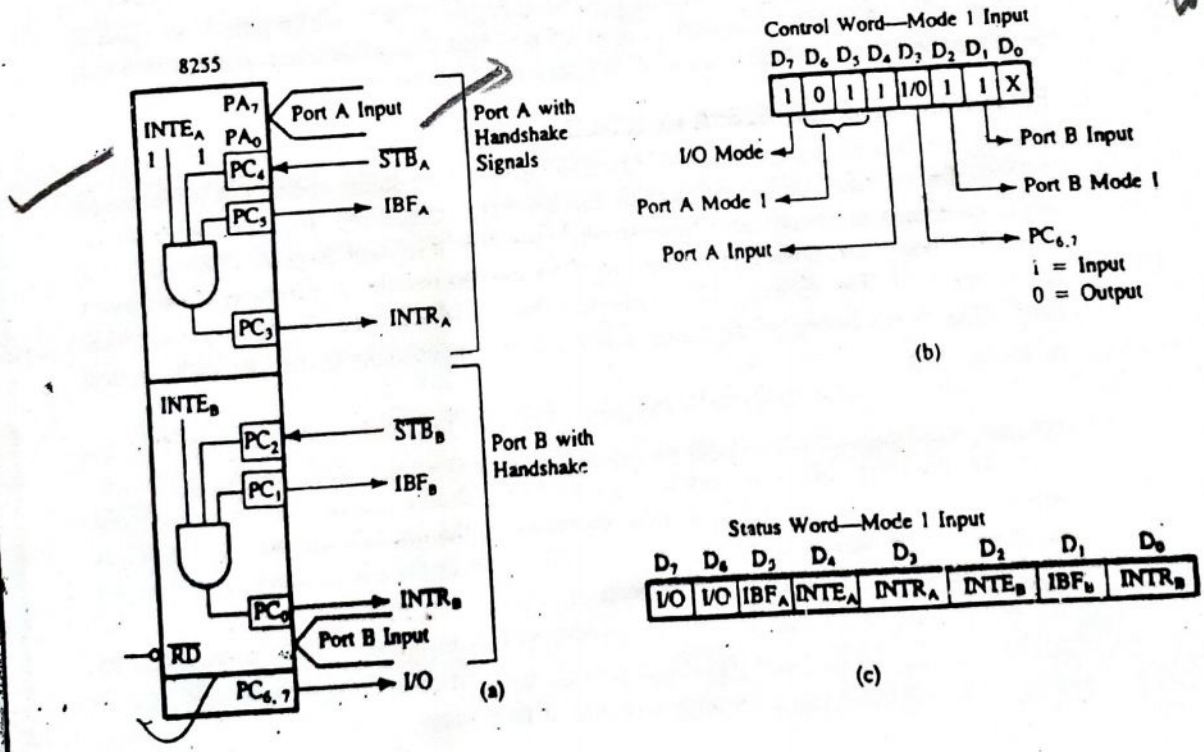



**FIGURE 15.8**
8255A Mode 1: Input Configuration

SOURCE: Adapted from Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–110.

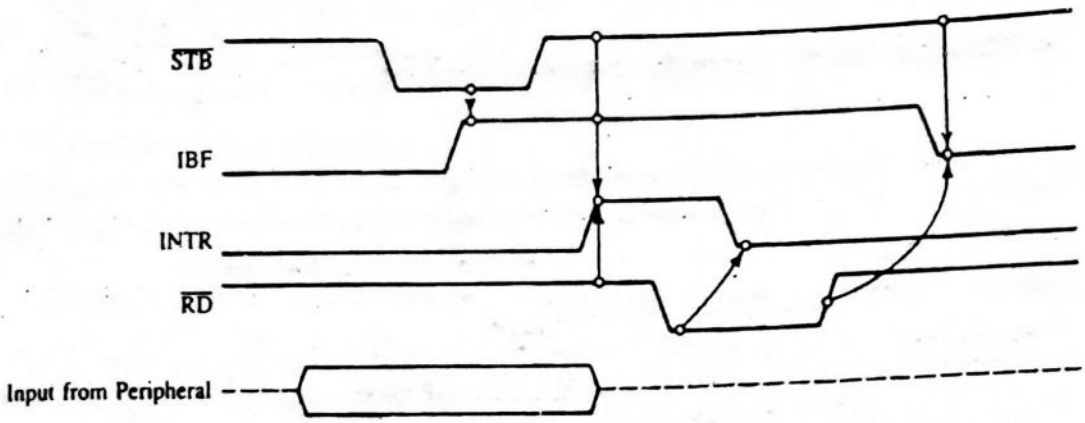



FIGURE 15.9
8255A Mode 1: Timing Waveforms for Strobed Input (with Handshake)
SOURCE: Adapted from Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–110.

- **INTE (Interrupt Enable):** This is an internal flip-flop used to enable or disable the generation of the INTR signal. The two flip-flops $INTE_A$ and $INTE_B$ are set/reset using the BSR mode. The $INTE_A$ is enabled or disabled through $PC_4$, and $INTE_B$ is enabled or disabled through $PC_2$.

## CONTROL AND STATUS WORDS

Figure 15.8(b) uses control words derived from Figure 15.4 to set up port A and port B as input ports in Mode 1. Similarly, Figure 15.8(c) also shows the status word, which will be placed in the accumulator if port C is read.

## PROGRAMMING THE 8255A IN MODE 1

The 8255A can be programmed to function using either status check I/O or interrupt I/O. Figure 15.10(a) shows a flowchart for the status check I/O. In this flowchart, the MPU continues to check data status through the IBF line until it goes high. This is a simplified flowchart; however, it does not show how to handle data transfer if two ports are being used. The technique is similar to that of Mode 0 combined with the BSR mode. The disadvantage of the status check I/O with handshake is that the MPU is tied up in the loop.

The flowchart in Figure 15.10(b) shows the steps required for the interrupt I/O, assuming that vectored interrupts are available. The confusing step in the interrupt I/O is to set INTE either for port A or port B. Figure 15.8(a) shows that the $\overline{STB}$ signal is connected to pin $PC_4$ and the $INTE_A$ is also controlled by the pin $PC_4$. (In port B, pin $PC_2$ is used for the same purposes.) However, the $INTE_A$ is set or reset in the BSR mode and the BSR control word has no effect when ports A and B are set in Mode 1.

In case the INTR line is used to implement the interrupt, it may be necessary to read the status of $INTR_A$ and $INTR_B$ to identify the port requesting an interrupt service and to determine the priority through software, if necessary.

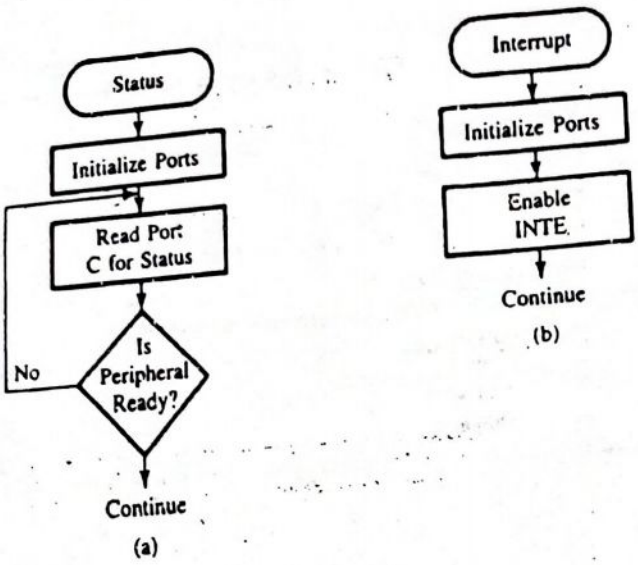



FIGURE 15.10
Flowcharts: Status Check I/O (a) and Interrupt I/O (b)

## MODE 1: OUTPUT CONTROL SIGNALS

Figure 15.11 shows the control signals when ports A and B are configured as output ports. These signals are defined as follows:

- **OBF (Output Buffer Full):** This is an output signal that goes low when the MPU writes data into the output latch of the 8255A. This signal indicates to an output peripheral that new data are ready to be read (Figure 15.12). It goes high again after the 8255A receives an $\overline{\text{ACK}}$ from the peripheral.
- **$\overline{\text{ACK}}$ (Acknowledge):** This is an input signal from a peripheral that must output a low when the peripheral receives the data from the 8255A ports (Figure 15.12).
- **INTR (Interrupt Request):** This is an output signal, and it is set by the rising edge of the $\overline{\text{ACK}}$ signal. This signal can be used to interrupt the MPU to request the next data byte for output. The INTR is set when $\overline{\text{OBF}}$, $\overline{\text{ACK}}$, and INTE are all one (Figure 15.12) and reset by the falling edge of $\overline{\text{WR}}$.
- **INTE (Interrupt Enable):** This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops $\text{INTE}_A$ and $\text{INTE}_B$ are controlled by bits $\text{PC}_6$ and $\text{PC}_2$, respectively, through the BSR mode.
- **$\text{PC}_{4,5}$:** These two lines can be set up either as input or output.

### CONTROL AND STATUS WORDS

Figure 15.11(b) shows the control word used to set up ports A and B as output ports in Mode 1. Similarly, Figure 15.11(c) also shows the status word, which will be placed in the accumulator if port C is read.

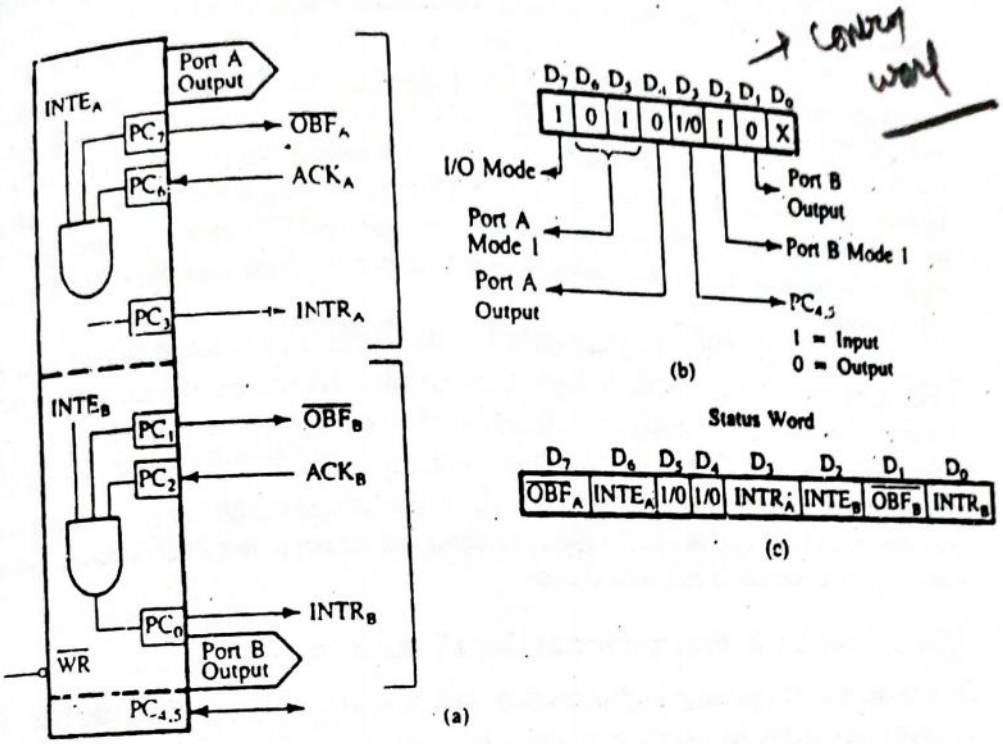



FIGURE 15.11
8255A Mode 1: Output Configuration
SOURCE: Adapted from Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–111.

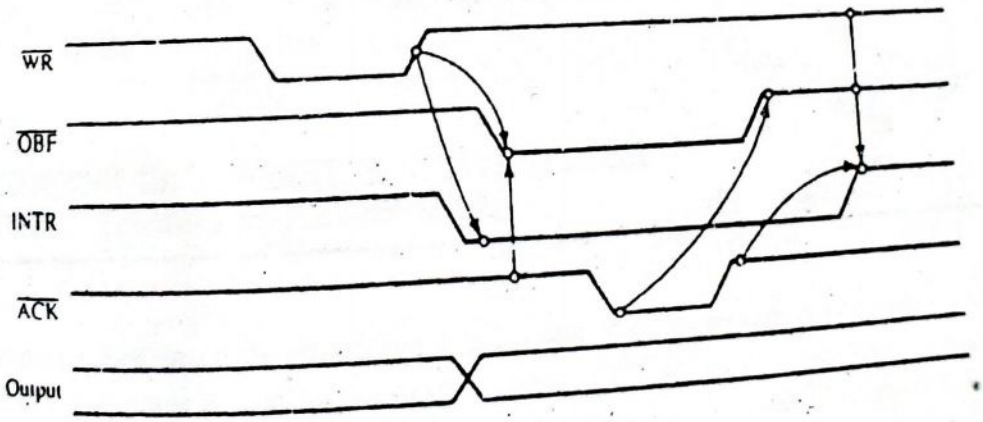



FIGURE 15.12
8255 Mode 1: Timing Waveforms for Strobed (with Handshake) Output
SOURCE: Adapted from Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3–111.

### 15.1.6 Illustration: An Application of the 8255A in the Handshake Mode (Mode 1)

PROBLEM STATEMENT

Figure 15.13 shows an interfacing circuit using the 8255A in Mode 1. Port A is designed as the input port for a keyboard with interrupt I/O, and port B is designed as the output port for a printer with status check I/O.