CHAPTER 19

8253

19.1 Introduction

Q. Write short note on 8254, Programmable interval timer.

In Microprocessor Based System, we come across two important modes i.e. timer → to provide delay and counter → to count incoming pulses. Presently, the way we implement timer/counter in 8086 based system as studied in earlier has following drawbacks :

(i) **Delay :** The 8086 can provide delays of any value, but it uses software to implement the delay. The instructions are arranged to waste time. The main disadvantage of this scheme is 8086 is executing some instructions, it means that it is busy in doing work.

(ii) **Counter :** The 8086 can count number of pulses arriving at port. To implement this 8086 goes on checking port, if it is active it increments counter by 1 and again goes on checking port. **The same disadvantage, 8086 will have to execute instructions.**

In large systems, where 8086 wastage time is critical, a separate timer IC 8254 can be used. The 8254 consists of 3 identical 16 bit counters. These counters can work as counter or can provide accurate time delays. To operate as a counter, a 16 bit count is loaded and the desired mode of operation is selected. The counters will work independently and generate the desired output. Now the 8086 job is to initialise and load counters.

In this chapter, we will discuss 8254 IC. Unless and until it is specified for 8253, the discussion of all points remains same in all respects to both ICs.

The two IC's 8253 and 8254 are timer ICs. Both are similar except following differences :

Q. How does 8254 differ from 8253 ?

8253	8254
1. Operating frequency 0 - 2.6 MHz.	Operating frequency 0 - 10 MHz.
2. Uses N-MOS technology.	Uses H-MOS technology.
3. Read-Back command is not available.	Read-Back command is available.
4. Reads and writes of the same counter cannot be interleaved.	Reads and writes of the same counter can be interleaved.

19.2 Features of Programmable Interval Timer

- Three independent 16 bit down counters.
- Counters can be programmed in 6 different programmable counter modes.
- Counting facility in both binary or BCD number system.
- Compatible with Intel and other microprocessors.
- Single + 5V supply.
- 24 pin dual in-line package.
- It is completely TTL compatible.
- It has a powerful command called READ BACK COMMAND which allows the user to check the count value, programmed mode and current mode and the current status of the counter (Only for 8254).
- Operating frequency range; For 8253 - DC to 2.6 MHz; For 8254 - DC to 10 MHz.

19.3 Pin Configuration of 8254

Q. Draw and explain the pin configuration of 8254.

The pin configuration of 8254 programmable interval timer is as shown in Fig. 19.3.1

$D_7 - D_0$	I/O	DATA BUS
CLK_N	I	Counter inputs
$GATE_N$	I	Counter gate inputs
OUT_N	O	Counter outputs
$\overline{RD}$	I	Read
$\overline{WR}$	I	Write
$\overline{CS}$	I	Chip select
$A_0 - A_1$	I	Counter select
V_{CC} / GND	I	+ 5 V supply/Ground

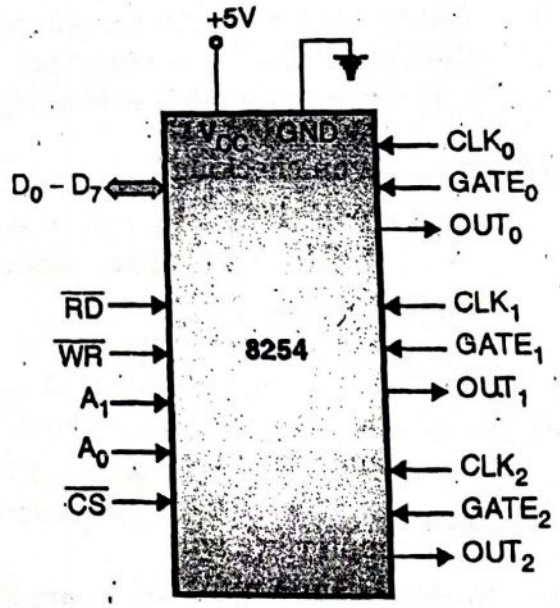


Fig. 19.3.1 : Pin diagram of 8254

Pin Description

Sr. No	Symbol	Name and function
1	D_0-D_7	**Data bus :** These are 8 bit bidirectional data bus lines, connected to the system data bus for data transfer between 8086 and 8254.
2	$\overline{CS}$	**Chip select :** This is an active low input signal, used to select the 8254 IC. If $\overline{CS}$ = 0 then 8254 will be active and take part in data transfer from/to 8086, otherwise 8254 will be in deactive state.

Sr. No	Symbol	Name and function
3	$\overline{RD}$	**Read :** This is an active low input signal, used in coordination with A_0 , A_1 to send data from appropriate counter to data lines D_0 - D_7.
4	$\overline{WR}$	**Write :** This is an active low input signal, used in coordination with A_0 , A_1 to load counters or to initialize counters.
5	A_0 - A_1	**Address lines :** These are input address lines used to distinguish different parts of 8254 such as Counter 0, Counter 1, Counter 2, Control word register.
6	CLK_{0-2}	**Clock input :** These are clock inputs to 3 independent counters. The pulses applied at these pins will be counted by respective counters.
7	$GATE_{0-2}$	**Gate control :** These are active high, input signals used to allow external hardware to control the respective counter. The function of gate input is dependent on operating mode.
8	OUT_{0-2}	**Output :** These lines are active high, output lines. The output is dependent on operating mode.

A_1	A_0	Selected part
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word register

19.4 8254 Functional Block Diagram

Q. Explain 8254 with its functional block diagram.

The block diagram of 8254 is as shown in Fig. 19.4.1.

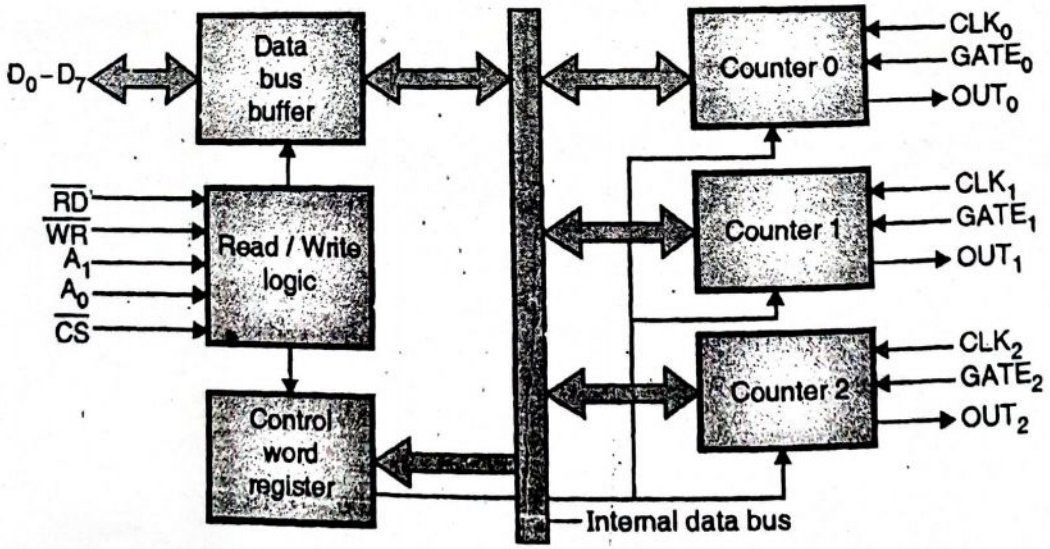


Fig. 19.4.1 : Functional block diagram of 8254

It includes data bus buffer, read/write logic, control word register and counters 0, 1, 2.

Data bus buffer

- It is tristate, bi-directional 8 bit data bus buffer.
- It is used to interface 8254 data bus with system data bus.
- It is internally connected to internal data bus and its outer pins D_0 - D_7 are connected to system data bus. The direction of data buffer is decided by read and write control signals.

Read/Write logic

- This block accepts inputs from system control bus and address bus.
- In I/O mapped I/O, the signals $\overline{RD}$ and $\overline{WR}$ are connected to $\overline{IOR}$ and $\overline{IOW}$.
- In memory mapped I/O, $\overline{RD}$ and $\overline{WR}$, are connected to $\overline{MEMR}$ and $\overline{MEMW}$.
- A_0 and A_1 are directly connected to address lines A_0 and A_1.
- $\overline{CS}$ is connected to address decoder.
- The 8254 operation/selection is enabled/disabled by $\overline{CS}$ signal. A_0, A_1 selects a specific part $\overline{WR}$, $\overline{RD}$ decides writing data to 8254 or reading data from 8254.
- The control word registers and the counters are selected according to the signals on lines A_0 and A_1.

A_1	A_0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word register

3) Control word register

- This register of 8254 gets selected when $A_0 = 1$ and $A_1 = 1$.
- It is used to specify the BCD or binary counter to be used, its mode of operation and the data transfer to be used i.e. read or write the data bytes (LSB, MSB or both).
- If the CPU performs a write operation, the data is stored in the control word register and is referred to as Control Word. It is used to define counter operation.
- The data can only be written into control word register, no read operation is allowed. Status information is available with the help of Read Back Command.

4) Counters

- There are three independent, 16 bit down counters.
- They can be programmed separately through control word register to decide mode of counter.

8253

- Each counter is having 2 inputs viz. CLK and GATE.
- CLK is used as an input to counter and GATE is used to control the counter.
- The counters give output on OUT pin.
- The loaded count value in counter will be decremented by counter at each clock input pulse. The programmer can read counter without disturbing counter operation.

19.5 Control Word Register Format

Q. Explain the control word register format of 8254.

- The control word register format is as shown in Fig. 19.5.1.

Note : $SC_0 = 1$ and $SC_1 = 1$, this combination is used to give read back command (Only for 8254).

i) The control word register bits, SC_1 and SC_0, select the control word register for counter. When $SC_0 = 0$ and $SC_1 = 0$, the control word for counter 0 is selected. Similarly, other counter control words, are selected by SC_0 and SC_1 and used to initialize the counters. A_0 and A_1 selects counter(s), but they are used to read/load counters by microprocessor.

ii) The bits RL_0 and RL_1 are used to read/load, data bytes i.e. LSB byte, MSB byte or both LSB and MSB bytes.

iii) The bits M_2, M_1 and M_0 decides the mode of operation for selected counter, Mode0 - Mode5.

iv) The bit, BCD, decides the mode of counting i.e. BCD counter or binary counter.

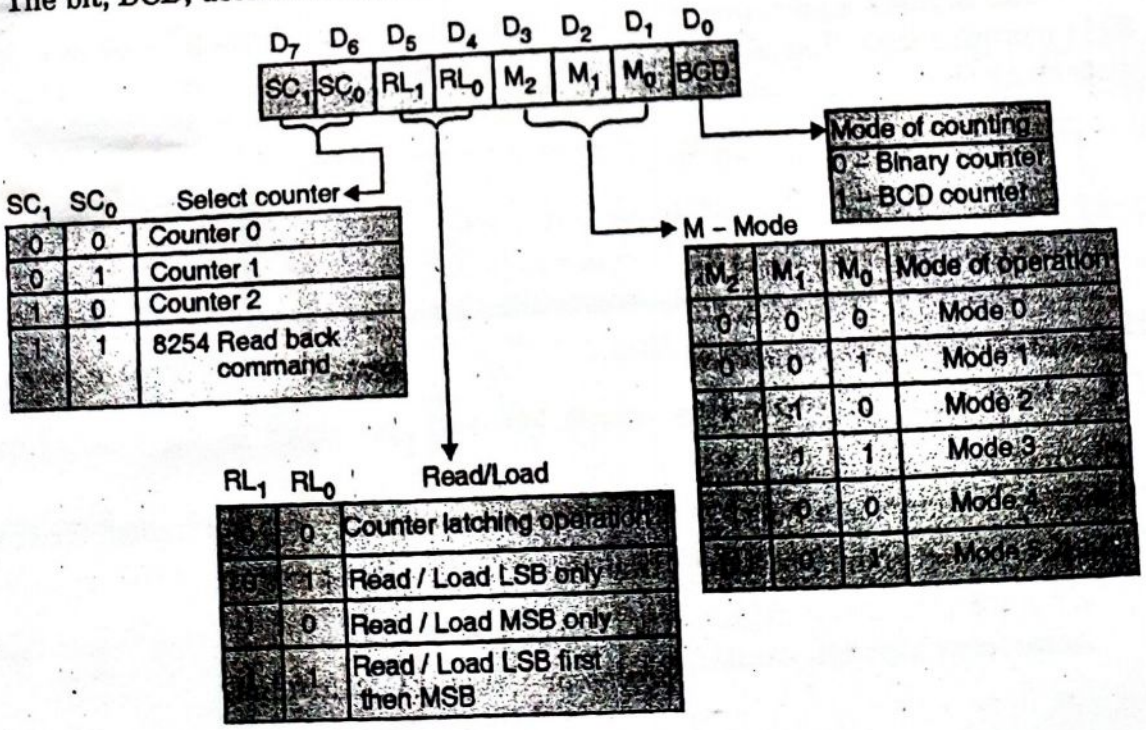


Fig. 19.5.1 : Control word register format

19.6 8254 Write Operation

The 8254 initialisation and count value loading operations are important operations performed by system software. Once 8254 is programmed it is ready to perform operations. The order of initialisation and count value loading for counter 0, counter 1 and counter 2 are sequence independent. But the number of data bytes programmed by RL_0 and RL_1 must be completed. The example format for this is as follows :

Sr. No.	A_1	A_0	
1	1	1	Control word register for counter 0
2	0	0	LSB count for counter 0
3	0	0	MSB count for counter 0
4	1	1	Control word register for counter 1
5	0	1	LSB count for counter 1
6	0	1	MSB count for counter 1
7	1	1	Control word register for counter 2
8	1	0	LSB count for counter 2
9	1	0	MSB count for counter 2

In above format, all the 3 counters are used with 16 bit count values.

Interleaved read and write

The special feature of 8254 is that the read and write operation of any counter may be interleaved. This feature allows us to read LSB byte then write LSB byte and read MSB byte then write MSB byte.

19.7 8254 Read Operations

The counter application, requires reading the value of the counter in progress. The 8254 contains logic that allows the programmer to read the contents of counters without disturbing the actual count in progress. There are 3 methods for 8254 as follows :

- Method 1 : Simple Read
- Method 2 : Counter Latch Operation
- Method 3 : Read Back Command (Only for 8254)

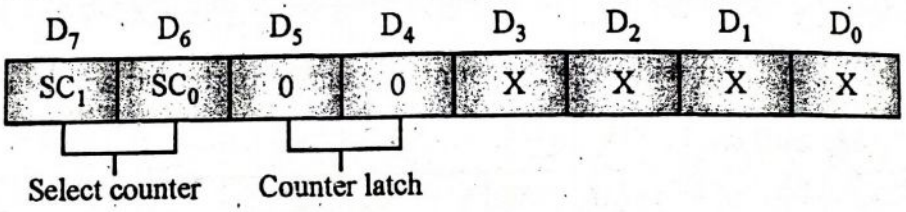
19.7.1 Method 1 : Simple Read

- The method 1 involves, the simple I/O read operations for the selected counter by using A_0, A_1 address inputs.
- The precaution should be taken that the RL_0- RL_1 bits programmed for reading the number of data bytes is followed.
- To perform the operation microprocessor issues $\overline{RD}$ control signal and takes count value from selected counter.

- If two bytes are programmed to be read, then two bytes must be read, before any write operation to the same counter.
- The requirement of this method for stable count reading is the counter should be inhibited. Because if a counter is changing its state and in the mean time when you read the contents, the count value will not be correct. To avoid such conditions the counter can be inhibited either by controlling the gate input or by external logic that inhibits the clock input. For example if the current count is 0100H. You read the lower byte and get it as 00H. Before you read the higher byte a pulse is applied on CLKn pin and the counter decrements i.e. it becomes 00FFH. Now when you read the upper byte, you get it as 00H. Hence the count you read is 0000H, which is incorrect, 0100H or 00FFH was correct.

19.7.2 Method 2 : Counter Latch Operation

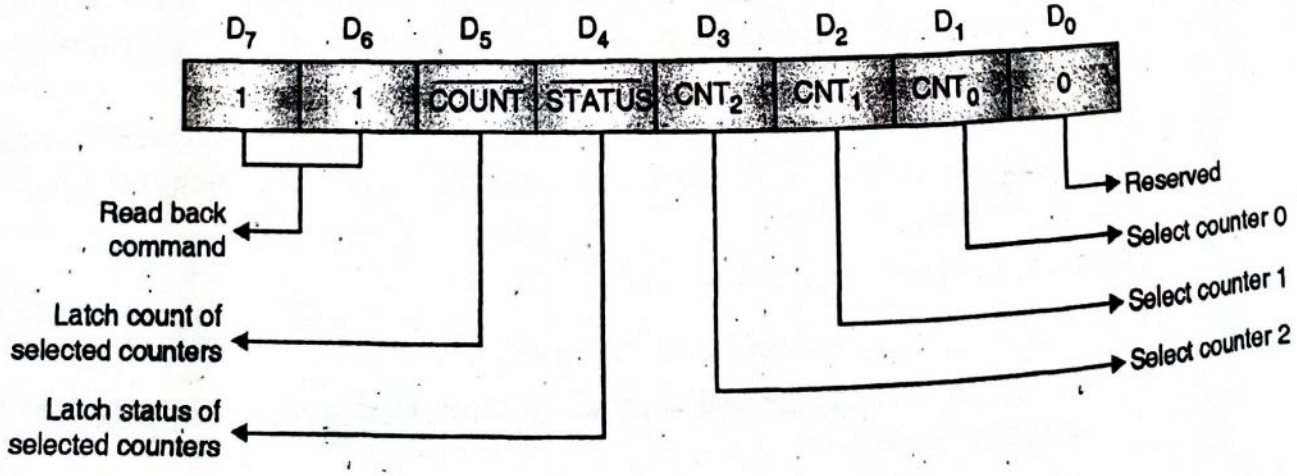
- The problem with the method 1 is, there are chances of reading incorrect count. To avoid this the 8254 provides counter latch operation. (RL_1 RL_0 = 00)
- The control word format for latching counter is as follows :



- When the above format is loaded in control register, it will latch the count value at that instant into special register.
- The contents of special register will be an accurate and stable quantity at that instant.
- The programmer then gives normal read commands to counter same as method 1 and contents of the latched register will be available. This type of reading count value contents is also called as ***reading on fly***.

19.7.3 Method 3 : Read Back Command (Only for 8254)

- In this method to get a stable count a counter is latched with a read back command. The format for read back command word is as follows :



In above control word format, when D_7 and D_6 bits of control word registers are 1, it is a read back command. The definition of other bits also changes as follows :

D_5 - latch count of selected counters.

D_4 - latch status of selected counters.

$D_3 D_2 D_1$ - select counter.

The advantage of this method is, you can latch one, two or all the three counters by putting 1 in the appropriate select counter bits. Once the counters are latched, the reading is performed by simple I/O read operation same as method 1.

The status word available, when a status is latched will be as follows :

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output	Null count	RL_1	RL_0	M_2	M_1	M_0	BCD

D_7 - Output : This gives the logic level of OUT pin of selected counter when bit = 0, OUT pin is LOW bit = 1, OUT pin is HIGH.

D_6 - Null count : This bit gives the status of counter. If the counter is zero, this bit will be set. If counter is not zero, this bit will be reset.

D_5 and D_4 : RL_1, RL_0 gives status of read load count value

D_3, D_2, and D_1 : M_2, M_1 and M_0 - gives status of mode

D_0 : BCD gives status of counter mode

19.8 Operating Modes of 8254

Q. Write down the names of different modes of operation of 8253 timer (PIT).

The programmable timer IC provides following modes of operations.

- Mode 0 : Interrupt on Terminal Count
- Mode 1 : Programmable One Shot / Hardware Triggerable One Shot
- Mode 2 : Rate Generator / Pulse Generator
- Mode 3 : Square Wave Generator
- Mode 4 : Software Triggered Strobe
- Mode 5 : Hardware Triggered Strobe

19.8.1 Mode 0 : Interrupt on Terminal Count

Control word format required for mode 0, counter 0, Read / Load LSB data byte only and BCD counter will be,

0	0	0	1	0	0	0	1

= 11 H

The three cases are as shown in Fig. 19.8.1 and their details are as follows :

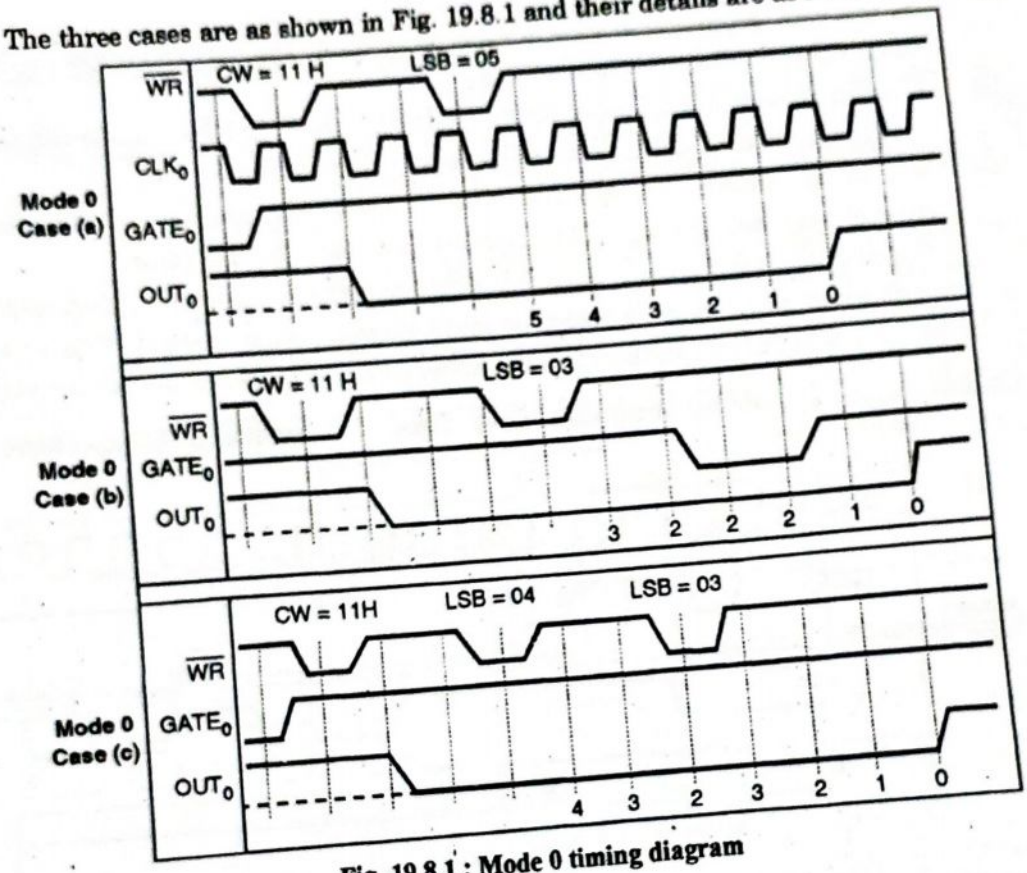


Fig. 19.8.1 : Mode 0 timing diagram

Case (a) : Normal operation

(i) The counter initialisation and loading operation is performed using two write operations. First write to load control word register for counter 0 (CWR = 11 H) and second to load count value (Data = 05 H). When counter is initialised in mode 0, the output goes LOW, at next negative going edge.

(ii) When the data 05 H is loaded, it is transferred to counter on next negative going edge of CLK_0 after $\overline{WR}$. Loading count value will start counter and counter will decrement count by 1 for each CLK_0 pulse.

(iii) When counter reaches zero the OUT_0 pin will go HIGH and remain HIGH. In case (a) we assume the status of GATE input is HIGH.

Case (b) : Gate disable

In this case counter operation is same as case (a). Only change is GATE input. If the GATE input becomes LOW the counter suspends counting. Again, when GATE becomes HIGH it will resume counting upto zero.

Case (c) : New count

In this case, counter operation is same as case (a). The only change is, loading new count value previous reaches to ZERO.

(i) If a new count value is loaded before counter reaches zero, the counter will take new count value and restart decrementing count value upto zero.

(ii) If a 16 bit counter (i.e. LSB and MSB) is used, then loading of LSBs, stops the current count and loading of MSB, restarts counter with new value.

The output in all 3 cases is made HIGH when count reaches zero. It remains HIGH until a new count value is loaded or mode of operation is changed. This output can be used as an interrupt, therefore the name given is ***Interrupt on terminal count.***

19.8.2 Mode 1 : Programmable One Shot / Hardware Triggerable One Shot

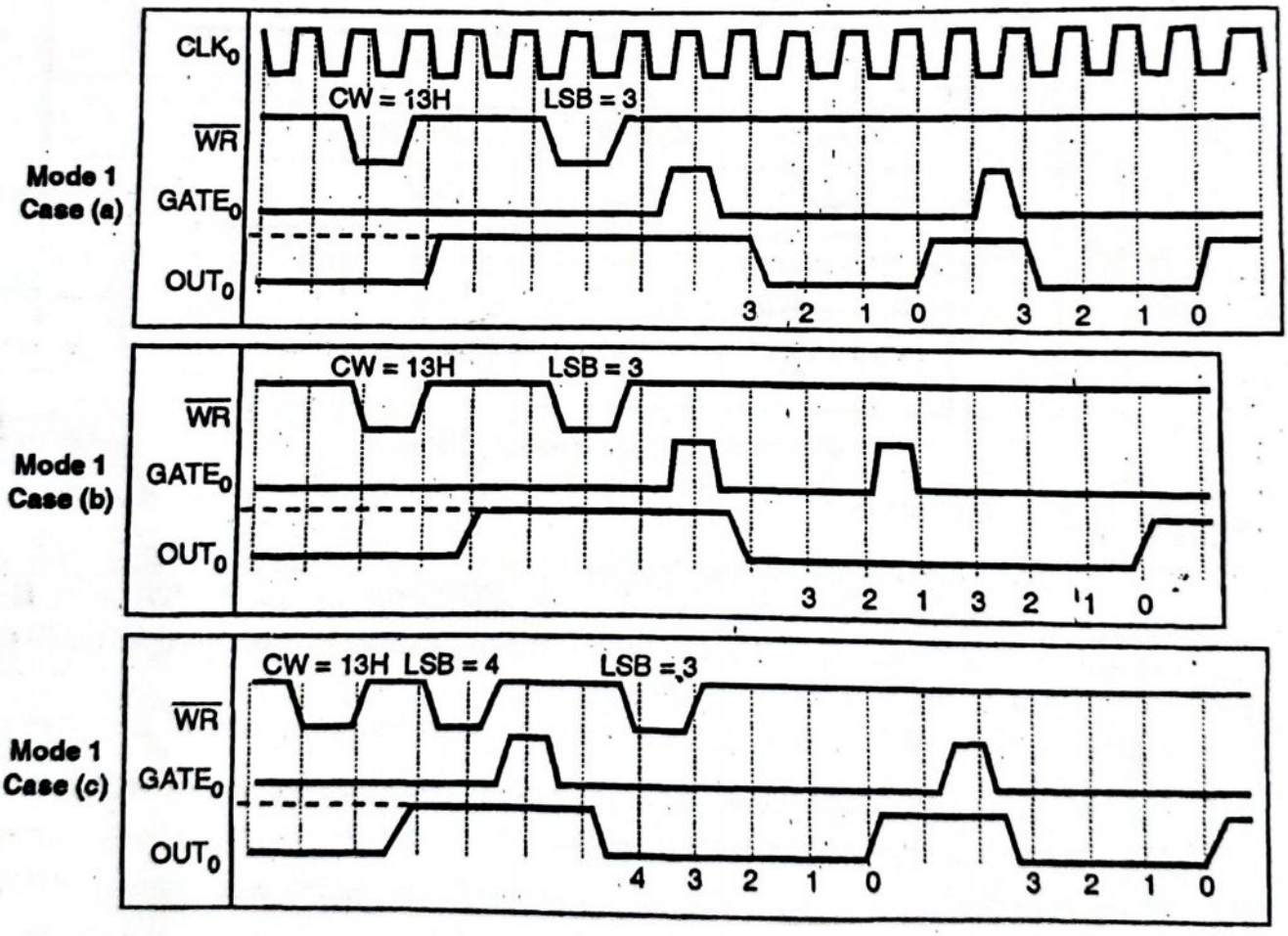


Fig. 19.8.2 : Mode 1 timing diagram

The control word format required for Mode 1, counter 0, Read / Load LSB data byte and BCD counter will be

0	0	0	1	0	0	1	1

= 13 H

The three cases are as shown in Fig. 19.8.2 and their details are as follows :