- Negative shifts are illegal.
- CL is default register used for rotate instruction when count is greater than 1.

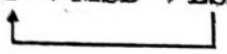
4. RCR – Rotate through carry right byte or word

Mnemonic RCR destination, count. **Flags** It affects only CF and OF

Algorithm Shift all bits right, the bit that goes off is set to CF and previous value of CF is inserted to the left most position

Addr. Mode Immediate addressing mode

Operation CF → MSB → LSB



- This instruction rotates all the bits is specified word or byte same number of bit positions to right. The destination can be register or memory location.
- Negative shifts are illegal.
- CL is default register used for rotate instruction when count is greater than 1.

12.9 Processor Control Instruction

Q. Explain control transfer and branching instruction of 8086.

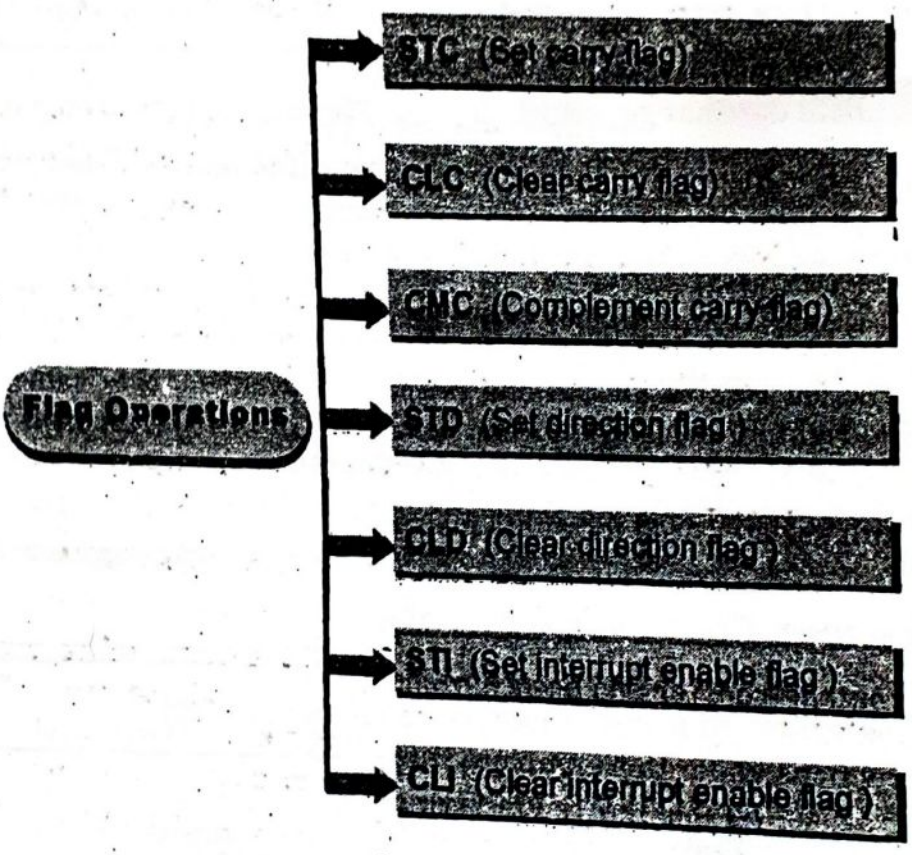
The instructions under this group are listed as follows :

Table 12.9.1 : Processor control instructions

FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
NO OPERATION	
NOP	No operation
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to external co-processor
LOCK	Lock bus during next instruction

These instructions allow programs to control various CPU functions. One group of instructions updates flags and another group is used primarily for synchronizing the 8086 or 8088 with external events. A final instruction causes the CPU to do nothing. Except for the flag operations, none of the processor control instructions affect the flags.

12.9.1 Flag Operations



1. CLC – Clear carry flag

Mnemonic CLC
Algorithm CF = 0
Addr. Mode Implied addressing mode
Operation CF ← 0 This instructions clears (resets) the carry flag to zero.
Flags Except carry, no other flags are affected.

2. STC – Set carry flag

Mnemonic STC
Algorithm CF = 1
Addr. Mode Implied addressing mode
Operation This instruction sets the carry flag.
Flags Except carry no other flags are affected.

3. CMC – Complement carry flag

Mnemonic CMC
Algorithm if CF = 0 then CF = 1 if CF = 1 then CF = 0
Flags Except carry no other flags are affected.

Addr. Mode Implied addressing mode

Operation $CF = \overline{CF}$ This instruction inverts the value of carry flag

4. CLD – Clear direction flag

Mnemonic CLD **Flags** Except direction flag, no other flags are affected.

Algorithm DF = 0

Addr. Mode Implied addressing mode

Operation

- It resets (DF) direction flag to zero. If the direction flag is reset, SI and / or DI will be automatically incremented during string operations.
- When one of the string instructions like MOVS, CMPS or SCAS executes it automatically increments the SI and / or DI registers.

5. STD – Set direction flag

Mnemonic STD **Flags** Except Direction no other flags are affected.

Algorithm DF = 1

Addr. Mode Implied addressing mode

Operation

- It is used to set the direction flag, so that SI and / or DI will be decremented by string instructions. i.e. CMPSB, MOVSB, STOSB, STOSW etc.

6. CLI – Clear interrupt enable flag

Mnemonic CLI **Flags** Except interrupt flag, it does not affect any other flag.

Algorithm IF = 0

Addr. Mode Implied addressing mode

Operation

- This instruction resets the interrupt flag to zero. No other flags are affected. If the interrupt flag is reset, the 8086 will not respond to an interrupt signal on its INTR input.
- This instruction has no effect on the NMI.

7. STI – Set interrupt enable flag

Mnemonic STI **Flags** Except interrupt flag, it does not affect any other flag.

Algorithm IF = 1

Addr. Mode Implied addressing mode

Operation

- This interrupt sets the interrupt flag to 1. This enables INTR interrupt of the 8086.

12.9.2 No Operation

Flags It does not affect any flag.

Mnemonic NOP

NOP : No operation

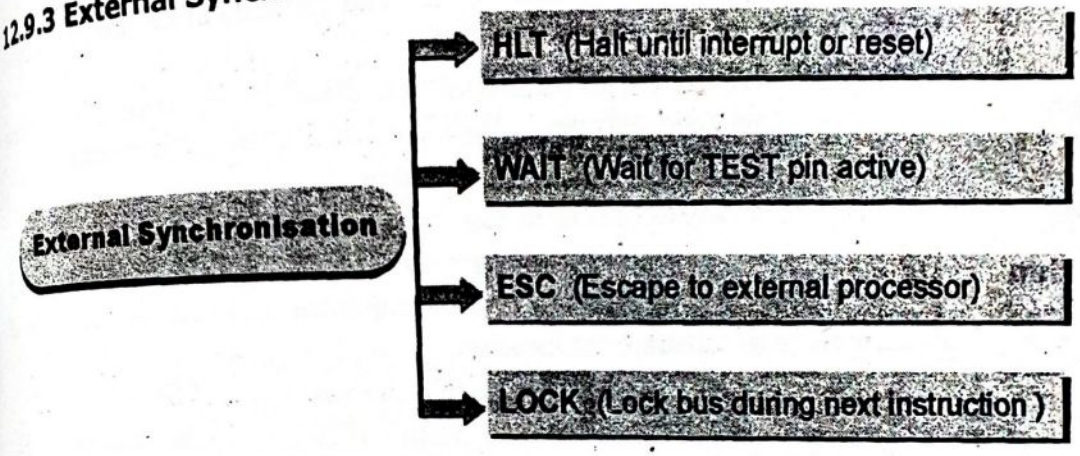
Algorithm Do nothing

Addr. Mode Implied addressing mode

Operation The execution of this instruction causes the CPU to do nothing.

- This instruction causes the CPU to do nothing. This instruction uses three clock cycles and increments the instruction pointer to point to the next instruction.
- It can be used to increase the delay of a delay loop.

12.9.3 External Synchronisation



1. HLT – Halt until interrupt or reset

Mnemonic Halt processing **Flags** No flags are affected.

Operation

- The HLT instruction will cause the 8086 to stop fetching and executing instructions. The 8086 enters into a halt state. To come out of the halt state, there are 3 ways given below.
  (i) Interrupt signal on INTR pin (ii) Interrupt signal on NMI pin
  (iii) Reset signal on reset pin.
- It may be used as an alternative to an endless software loop in situations where a program must wait for an interrupt.

2. WAIT – Wait for TEST pin active

Mnemonic WAIT

Operation **Flags** No flags are affected.

When this instruction executes, the 8086 enters on idle condition in which it is doing no processing.

- The 8086 will stay in this idle state until 8086 $\overline{\text{TEST}}$ input pin is made low or on interrupt signal is received on the INTR or NMI interrupt pins.