What does an offset tell us ?

- The offset is a 16 bit hex number contained by the instruction pointer (I.P.) register and it tells BIU the location in the code segment, from which the next instruction byte is to be fetched.

11.6 Pin Diagram of 8086

Sr. No.	Pins	Name of the pins
1.	Supply pins (3 pins)	V_{CC} GND GND
2.	Clock related pins (3 pins)	CLK RESET READY
3.	Address and Data pins (21 pins)	$AD_0 - AD_{15}$ $A_{16}/S_3 - A_{19}/S_6$ $\overline{BHE}$ / S_7
4.	Interrupt pins (2 pins)	NMI INTR
5.	Other control (3 pins)	$\overline{TEST}$ MN / $\overline{MX}$ $\overline{RD}$
6.	Mode multiplexed signals (8 pins) (MIN mode – MAX mode signals)	HOLD – $\overline{RQ_0}$ / $\overline{GT_0}$ HLDA – $\overline{RQ_1}$ / $\overline{GT_1}$ $\overline{WR}$ – $\overline{LOCK}$ $\overline{DEN}$ – $\overline{S_0}$ DT / $\overline{R}$ – $\overline{S_1}$ M / $\overline{IO}$ – $\overline{S_2}$ ALE – QS_0 $\overline{INTA}$ – QS_1

I. Supply pins (3 pins)

V_{CC}	GND	GND

- Used for power supply i.e. +5V on V_{CC} w.r.t. GND.
- Two separate GND pins for two layers of 8086 chip, improves the noise rejection.

II. Clock related pins (3 pins)

CLK	RESET	READY

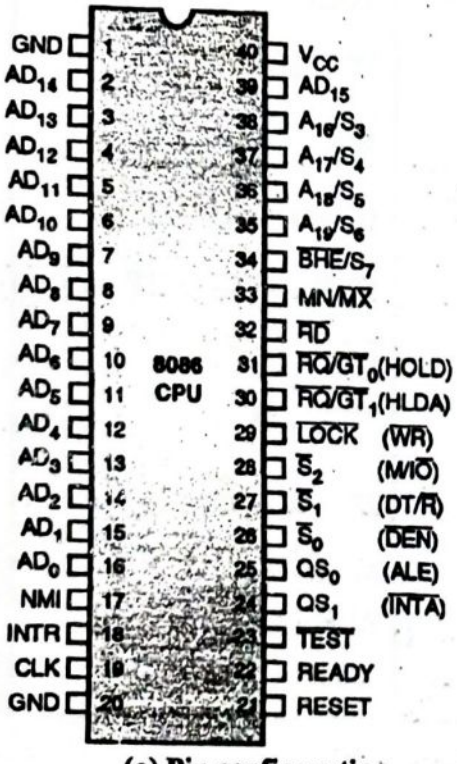
CLK

- This pin provides the basic timing for the processor.
- 8086 does not has an on-chip clock generator hence an external clock generator like 8284 is used to provide the clock signal.
- It is asymmetric with 33% duty cycle, TTL clock signal.

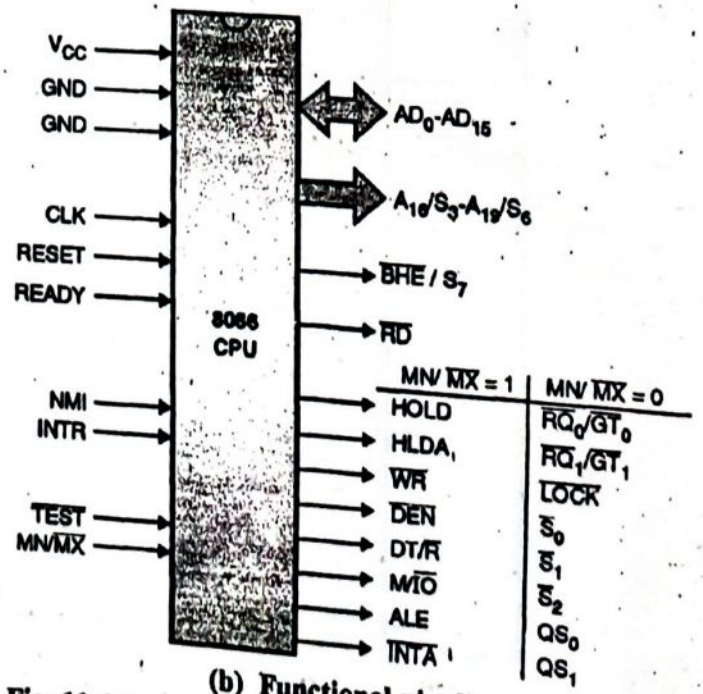
RESET

- It causes the processor to immediately terminate its present activity. The 8284 clock generator provides this signal.
- This signal must be active high for atleast 4 clock cycles
- It clears all the flag register, the Instruction Queue, the DS, SS, ES and IP registers and sets the bits of CS register.
- Hence the reset vector address of 8086 is FFFF0H (as CS = FFFFH and IP = 0000H).

READY



(a) Pin configuration



(b) Functional pin diagram

Fig. 11.6.1

- It is an acknowledgement from the addressed memory or I/O that it will complete the data transfer specially meant for slow devices.
- µP samples the READY input between T2 and T3 of a M/C cycle.
- If READY pin is LOW, µP inserts wait-states between T2 and T3, until READY becomes HIGH.

III. Address and data pins (21 pins)

$AD_{15} - AD_0$	$A_{16}/S_3 \ldots A_{19}/S_6$	$\overline{BHE}/S_7$

$AD_{15} - AD_0$

- These are time multiplexed data address lines i.e. for some time they have address and for some time data
- It gives the address $A_{15} - A_0$ during T1 of an Machine Cycle. (When ALE = 1)
- It gives the data $D_{15} - D_0$ after T1 of an M/C Cycle (Machine cycle).

$A_{16}/S_3 \ldots A_{19}/S_6$

- These lines work as Address bus ($A_{16} \ldots A_{19}$) during T1 of every M/C Cycle.
- T2 onwards these lines work as Status signals $S_3 \ldots S_6$.
- S_3 and S_4 gives the status of the memory segment currently accessed. S_6 gives the status of the Interrupt Enable Flag updated every clock cycle. S_6 goes low when 8086 controls the shared system bus.

S_4	S_3	Segment accessed
0	0	Extra Segment
0	1	Stack Segment
1	0	Code Segment or None
1	1	Data Segment

$\overline{BHE}/S_7$ Bus High enable

- This line carries the $\overline{BHE}$ signal during T1.
- $\overline{BHE}$ and A_0 are used together to access a word/byte from the memory as shown in the banking in section 11.8.
- Status line S_7 is reserved for "further development".

IV. Interrupt pins (2 pins)

NMI	INTR

NMI

- This is a non-maskable, edge triggered that causes type 2 interrupt i.e. on receiving an interrupt on NMI line, the µP executes INT 2 and transfers the control to location 2 * 4 =00008H in the Interrupt Vector Table (IVT). It reads 4

locations starting from this address to get values for IP and CS of the ISR address.

- It is not maskable internally by software.
- A transition from LOW to HIGH on this pin, causes the interrupt at the end of the current instruction

INTR

- This is a non-vectored, maskable, level triggered interrupt sampled during last clock cycle of each instruction.
- To get the vector number for the interrupt the following procedure is followed
- On receiving an interrupt on INTR line, the µP executes 2 $\overline{\text{INTA}}$ pulses.
- First $\overline{\text{INTA}}$ pulse → the interrupting device is indicated for its interrupt being accepted while the device calculates the vector number.
- Second $\overline{\text{INTA}}$ pulse → the interrupting device sends the vector number to the microprocessor on the data lines.
- Control shifts to location pointed by IP and CS which are loaded from IVT at Vector No * 4.

V. Other control (3 pins)

$\overline{\text{TEST}}$	MN/$\overline{\text{MX}}$	$\overline{\text{RD}}$

$\overline{\text{TEST}}$

- It is an active low input line dedicated for 8087 Co-processor.
- In minimum mode it is connected to GND. In Maximum Mode whenever the Co-processor is busy it makes this pin HIGH.
- $\overline{\text{TEST}}$ input is examined by the WAIT instruction.
- If the TEST pin is high, the µP enters idle state; till TEST pin becomes low i.e. 8087 is free.

MN/$\overline{\text{MX}}$

- This is an input signal to 8086 that indicates the processor has to work in which mode.
- If this signal is HIGH, 8086 is in Minimum mode i.e. Single-processor system.
- If this signal is LOW, 8086 is in Maximum mode i.e. Multiprocessor system.

$\overline{\text{RD}}$

- It is an active low output signal. When it is low 8086 reads from memory or an I/O device.

VI. Mode multiplexed signals (8 pins) (MIN Mode — Max Mode Signals)

HOLD — $\overline{RQ_0}/\overline{GT_0}$	HLDA — $\overline{RQ_1}/\overline{GT_1}$	$\overline{WR}$ — LOCK	$\overline{DEN}$ — $\overline{S_0}$
DT/$\overline{R}$ — $\overline{S_1}$	M/$\overline{IO}$ — $\overline{S_2}$	ALE — QS_0	$\overline{INTA}$ — QS_1

HOLD — $\overline{RQ_0}/\overline{GT_0}$

- In Minimum Mode this line carries the HOLD input signal from another master requesting a local bus.
- The DMA Controller issues the HOLD signal to request for the system bus.
- In response 8086 completes the current bus cycle and releases the system bus.
- In Maximum Mode it carries the bi-directional $\overline{RQ_0}/\overline{GT_0}$ (Request/Grant) signal.
- The external bus master (8089 or 8087) sends an active low pulse to request for the control over the system bus.
- In response the 8086 completes the current bus cycle, releases the system bus and sends an active low Grant pulse on the same line to the external bus controller.
- 8086 gets back the system bus only after external bus master sends an active low release pulse on the same line.

HLDA — $\overline{RQ_1}/\overline{GT_1}$

- In Minimum Mode, this line carries the HLDA signal.
- This signal is issued by 8086 after releasing the system bus.
- In Maximum Mode it functions as $\overline{RQ_1}/\overline{GT_1}$ which is the same as $\overline{RQ_0}/\overline{GT_0}$; but is of lower priority

$\overline{WR}$ — $\overline{LOCK}$

- In Minimum Mode this line carries the $\overline{WR}$ signal indicates a write operation when this pin is Low.
- It is used with M/$\overline{IO}$ to write to Memory or IO Device.
- In Maximum mode it functions as the $\overline{LOCK}$ output line.
- When 8086 executes an instruction with the LOCK prefix this signal is active (i.e. low) remains active till next instruction, indicating the external bus master cannot take control of the system bus.

$\overline{DEN}$ --- $\overline{S_0}$

- In Minimum Mode it carries the $\overline{DEN}$ signal and is used to enable the Data transceivers (bidirectional buffer IC 8286).
- In Maximum Mode it carries the $\overline{S_0}$ signal. $\overline{S_0}$ is a status signal given to 8288.
- In Maximum Mode, Bus Controller (IC 8288) generates the DEN signal for 8286.

DT/$\overline{R}$ --- $\overline{S_1}$

- In Minimum Mode it carries the DT/$\overline{R}$ signal indicating Data Transmit or Receive.
- This signal goes low for a read operation and high for a write operation.
- In Maximum Mode it carries the $\overline{S_1}$ signal. $\overline{S_1}$ is a status signal given to 8288.
- In Maximum Mode, Bus controller issues the DT/$\overline{R}$ signal to 8286..

M/$\overline{IO}$ --- $\overline{S_2}$

- In Minimum Mode it carries the M/$\overline{IO}$ signal, to distinguish between Memory and IO access.
- In Maximum Mode it carries the $\overline{S_2}$ signal. $\overline{S_2}$ is a status signal given to 8288.
- In Maximum Mode $\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$ are used to generate the appropriate control signal.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Machine cycle
0	0	0	Interrupt Acknowledge
0	0	1	Read I /O Port
0	1	0	Write I / O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

ALE --- QS_0

- In Minimum Mode it carries the ALE signal, which is used to demultiplex address data line by latching the address.
- In Maximum Mode it carries the QS_0 signal.
- It is used with QS_1 to indicate the Instruction Queue Status.
- In Maximum Mode, Bus Controller 8288 issues the ALE signal. (to Latch IC - 8282)

$\overline{INTA}$ --- QS_1

- In Minimum Mode it carries the $\overline{INTA}$ signal.
- It is issued in response to an interrupt on the INTR line.
- It is used to read the vector number form the interrupting device.
- In Maximum Mode it carries the QS_1 signal.
- In Maximum Mode, Bus Controller issues the $\overline{INTA}$ signal. (to 8086)

QS_1	QS_0	Queue Status
0	0	No Operation
0	1	First byte of Opcode from queue
1	0	Empty the Queue
1	1	Subsequent byte from queue

11.7 Intel 8088 Microprocessor

- The Intel 8088 processor is very similar to 8086 in many aspects. In this section we will discuss the pin diagram internal architecture and features of 8088.
- The internal architecture of 8086 is similar to that of 8086 but the external data bus of 8088 is only 8 bit ($D_7 - D_0$).

11.7.1 Internal Architecture of 8088

- The internal architecture of 8088 is as shown in Fig. 11.7.1. It shows that except the Queue every thing else is exactly same as that in 8086.
- The queue in 8088 is of 4 byte length instead of being 6 byte long like 8086.