2.4 Pin Functions

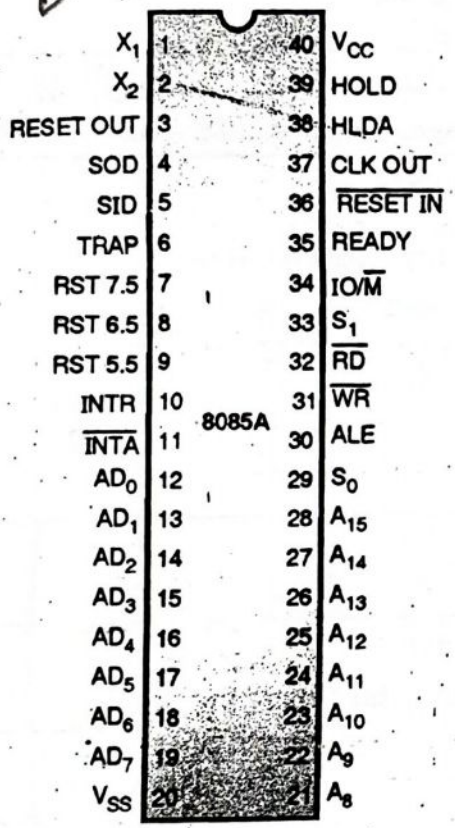

Fig. 2.4.1 : Pin diagram of 8085

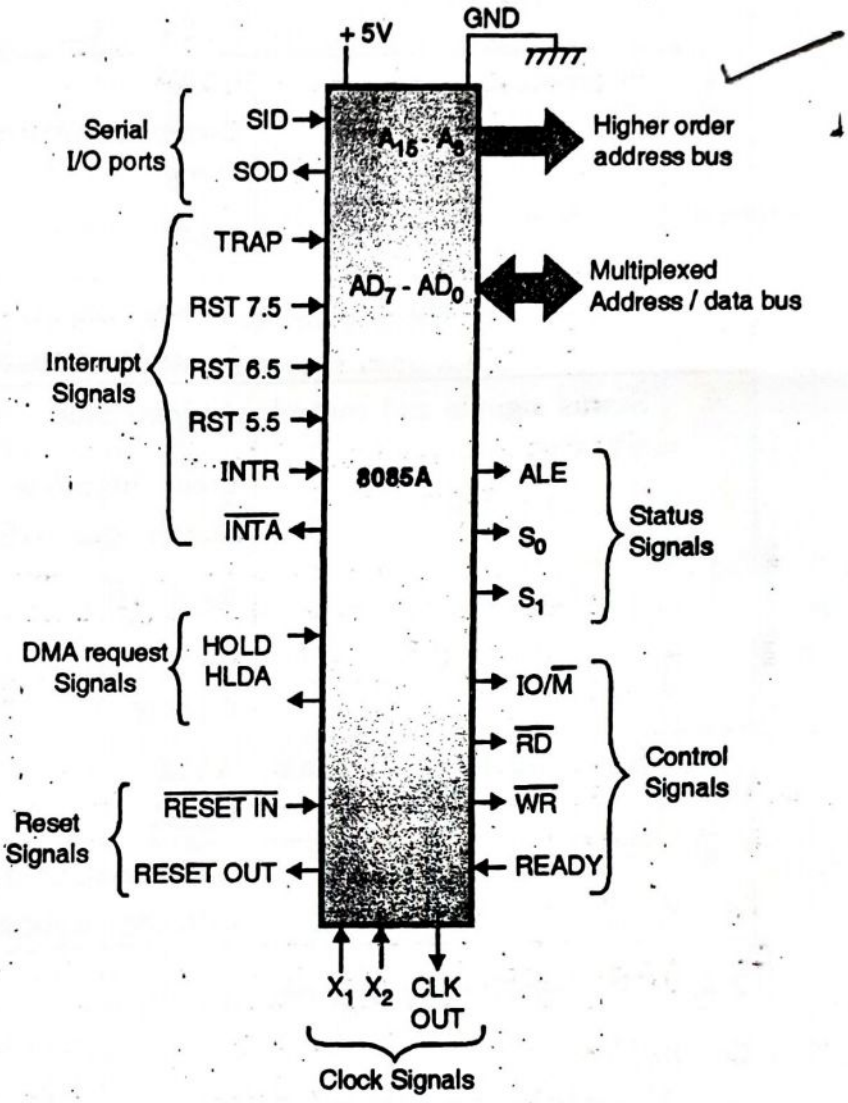

Fig. 2.4.2 : Groups of 8085 signals

The 8085A is an 8 bit general purpose microprocessor having 40 pins and works on single power supply. Fig. 2.4.1 shows the pin diagram of 8085A. To study the pin diagram we group the signals as shown in Fig. 2.4.2. They are as follows :

Sr. No.	Signals	Pins
1.	Power supply signals	V_{CC} V_{SS}
2.	Clock signals	X_1 X_2 CLK OUT

Sr. No.	Signals	Pins
3.	Reset signals	$\overline{\text{RESETIN}}$ RESET OUT
4.	Interrupt signals	TRAP Restart interrupts (RST 7.5, RST 6.5 and RST 5.5) INTR $\overline{\text{INTA}}$
5.	Address bus and data bus	Address bus ($A_8 - A_{15}$) Multiplexed address / data bus ($AD_0 - AD_7$)
6.	Status signals and control signals	Address latch enable (ALE) Input output/memory (IO/$\overline{\text{M}}$) Status signals (S_1 and S_0) Read ($\overline{\text{RD}}$) Write ($\overline{\text{WR}}$) READY
7.	Serial input/output signals	HOLD HLDA
8.	DMA request signals	SID (Serial input data) SOD (Serial output data)

2.4.1 Power Supply Signals

V_{CC} and V_{SS}

- V_{CC} is to be connected to + 5 V power supply.
- V_{SS} – Ground reference.

2.4.2 Clock Signals

(1) X_1 X_2

- These are clock input signals, connected to crystal, LC or RC network. The crystal, LC or RC is connected between these two pins.
- The X_1 and X_2 pins drive the internal clock generator circuit. Hence, externally only one crystal is enough.
- The frequency is divided by 2 and used as operating frequency. Generally the 6.014 MHz crystal is connected to X_1 and X_2, this is divided by 2. So the operating frequency of 8085 is 3.07 MHz.

(2) CLK OUT

- This is an output signal, used as a system clock.

- The internal operating frequency is available on CLK OUT pin.
- This pin can be used by the peripherals as a system clock input for t operation. Hence, there will be synchronization between the differ peripherals and the microprocessor.

2.4.3 Reset Signals

Q. What happens when 8085 CPU is reset ?

$\overline{\text{RESETIN}}$

- This is an active low, input reset signal. When $\overline{\text{RESETIN}}$ = 0, it clears progr counter i.e. 0000 and makes address, data and control lines tristated. After reset status of internal register and flags are unpredictable. The instruction registe reset. Halt flip-flop is reset. The program counter is reset. All maskable interru are disabled. Also, other peripherals alongwith 8085 are reset.
- The CPU is held in the reset condition as along as $\overline{\text{RESETIN}}$ is applied.
- After reset the microprocessor starts executing instructions from 0000 H onwards

RESET OUT

- This is an active high, output signal used to indicate that the microprocesso reset.
- This signal is used as system reset, to reset other devices connected in system.

2.4.4 Interrupt Signals

(1) TRAP

- This is an active high level and edge triggered, non maskable, vecto highest priority interrupt.
- When TRAP line is active microprocessor performs internal res automatically at vector address 0024 H.

(2) Restart interrupts (RST 7.5, RST 6.5 and RST 5.5)

- These are active high level, triggered, vectored, maskable interrupt. T
- cause an internal restart to be automatically inserted.
- The priorities of these are RST 7.5, RST 6.5, RST 5.5.
- When RST 7.5, RST 6.5 or RST 5.5 is active microprocessor perfo internal restart automatically at vector addresses 003C H, 0034 H, 002 respectively.

(3) INTR

- INTR is an active high, level triggered, general purpose, non-vecto interrupt.
- It has the lowest priority.
- Whenever a device requires a service it has to request service on this pi making it's logic "1".
- The interrupting device has to state where the interrupt service routin placed in the memory.

(4) $\overline{\text{INTA}}$

- It is an output signal.

- $\overline{INTA}$ is used to indicate that the microprocessor has received an INTR interrupt.

2.4.5 Address Bus and Data Bus

Q. Address bus is unidirectional. Justify this statement.

1) Address bus ($A_8 - A_{15}$)

- These are output, tristate signals used as higher order 8 bits of 16 bit address.
- The address bus is always unidirectional meaning that the address is given by 8085 to select a memory or an I/O location.
- It is used to identify a memory location or a peripheral device.

2) Multiplexed address/data bus ($AD_0 - AD_7$)

Q. 1 Why are the AD_0 - AD_7 lines multiplexed ?

Q. 2 What do you mean by multiplexed addressed data bus ?

Q. 3 What is the advantage and disadvantage of multiplexed bus ?

- These are input/output, tristate signals having two set of signals. They are address and data.
- The lower order 8 bits, of 16 bit address is multiplexed or time shared with data bus.
- They are demultiplexed with the help of ALE signal. During the earlier part it is used as lower order address and in later part it is used as data bus.
- The address and data buses are multiplexed to reduce the number of pins of the chip.

2.4.6 Status and Control Signals

Q. What are the main control signals used by 8085 ? Explain their function.

1) Address latch enable (ALE)

- This is an output signal, used to give information of $AD_0 - AD_7$ contents.
- It is a positive going pulse generated during the first clock cycle of a machine cycle.
- When pulse is high it indicates that the contents of $AD_0 - AD_7$ are address. When it is low it indicates that the contents are data.
- The ALE signal is used to separate $AD_0 - AD_7$ (i.e. demultiplex) to $A_0 - A_7$ and $D_0 - D_7$. To do this separation an external latch is connected to $AD_0 - AD_7$ lines and this latch is controlled by ALE signal.

2) Input output/memory ($IO/\overline{M}$)

- This is an output status signal, used to give information of operation to be performed with memory or I/O device.
- If $IO/\overline{M}$ = 0, the microprocessor is performing a memory related operation.
- If $IO/\overline{M}$ =1 the microprocessor is performing an I/O device related operation.

3) Status signals (S_1 and S_0)

- These are output status signals used to give information of operation performed by microprocessor.
- When S_0 and S_1 is combined with $IO/\overline{M}$ we get status of all the machine cycles (operations) performed by 8085 as shown in Table 2.4.1.

Table 2.4.1

Status Signals			Operation	Control signals used
$IO/\overline{M}$	S_1	S_0		
0	0	0	–	–
0	0	1	Memory write	$\overline{WR}$
0	1	0	Memory read	$\overline{RD}$
0	1	1	Opcode fetch	$\overline{RD}$
1	0	0	–	–
1	0	1	I/O write	$\overline{WR}$
1	1	0	I/O read	$\overline{RD}$
1	1	1	Interrupt acknowledge	$\overline{INTA}$
Z	0	0	Halt	–
Z	X	X	Hold	
Z	X	X	Reset	

Note : Z – Tristate (High impedance condition) X – Unspecified condition

4) Read ($\overline{RD}$)

- This is an active low signal.
- It is an output control signal that is used to read data from the selected memory location or an I/O location via the data bus.
- A low on this pin indicated that a operation performed is a read operation .

5) Write ($\overline{WR}$)

- This is an active low signal.
- It is an output control signal used to write data to selected memory location or an I/O location via data bus.

- A low on this pin indicated that a operation performed is a write operation.

6) READY

- This is an active high input control signal.
- It is used by microprocessor to detect whether a peripheral is ready for the data transfer or not. If not the processor waits till the signal goes high.
- The main function of this pin is to synchronize the microprocessor 8085 with slower peripherals. i.e. the microprocessor waits till the peripheral is not ready to accept/send the data.

2.4.7 DMA Request Signals

HOLD and HLDA

- HOLD is an active high, input signal used by other controller to request microprocessor about use of address, data and control signals.
- The Hold and HLDA signals are used for Direct Memory access (DMA).
- The DMA Controller receives a request from a device and in turn issues the HOLD signal to the microprocessor.
- The processor releases the system bus and then acknowledges the HOLD signal with HLDA signal. The DMA transfer thus begins.
- The DMA controller will use the buses. On completion of work will disable HOLD signal. Because of this microprocessor will also make HLDA low. The microprocessor takes control of buses half clock cycle after HLDA goes low.

2.4.8 Serial I/O Signals

Q. What is the use of SID and SOD pins of 8085 ?

(1) SID (Serial input data)

- This is an active high, serial input port pin, used to accept serial 1-bit data under software control.
- When a RIM instruction is executed the SID pin data is loaded in bit D_7 of accumulator.

(2) SOD (Serial output data)

- This is an active high, serial output port pin, used to transfer serial 1-bit data under software control.
- When a SIM instruction is executed the SOD pin is set or reset depending on D_7 and D_6 bits of accumulator.

2.5 Address, Data and Control Buses

Q. What are the types of buses ? Discuss 8085 microprocessor system buses.

- A set of pins, wires or signals having common function is called as bus.

- A bus is a bundle of wires that are grouped together to serve a single purpose in th 8085 microprocessor there are three sets of communication lines that are calle buses. They are the address bus, the data bus and control bus. The three buse together form the "**system bus**"
- Fig. 2.5.1 shows the 8085 bus structure.

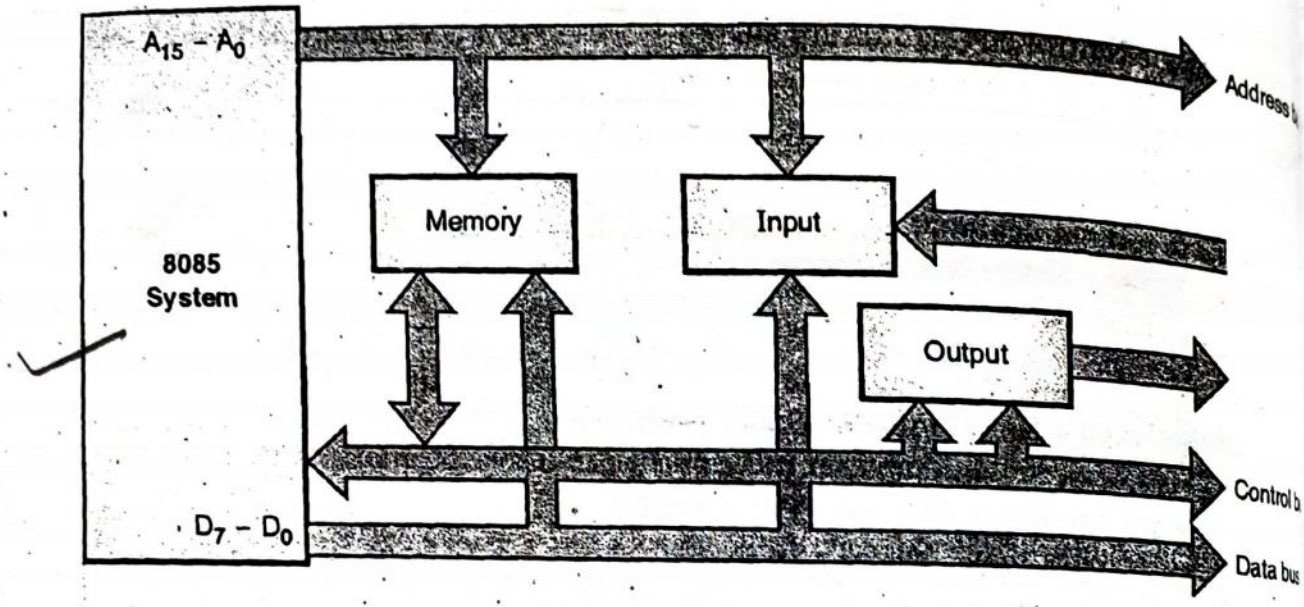

Fig. 2.5.1 : The 8085 bus structure

2.5.1 Address Bus

- The bus over which the microprocessor sends out the address of a memory loca or I/O location is called as the address bus.
- The address bus carries the address of the memory or I/O location to be rea written from.
- In 8085 the address bus is 16-bit ($A_0 - A_{15}$). So the microprocessor can be us access 16 bit address and is capable of addressing $2^{16} = 65536$ i.e. 64 K me locations.
- The address bus is unidirectional i.e. bits flow only in one direction from microprocessor unit to memory and I/O devices.
- The address bus is also used to send the port address on the address bus. Whe microprocessor reads data from or writes data to a port, it sends the port addre on the address bus.

2.5.2 Data Bus

- The data bus of 8085 consists of 8 parallel lines $D_0 - D_7$.
- The data bus is a bi-directional bus. This means the data can be transferred CPU to memory or I/O locations and viceversa.
- The number of data lines used in the data bus is equal to the size of data word written or read.
- The data bus also connects the I/O ports and microprocessor. So the micropro can write data to or read data from the memory or the I/O ports.

2.5.3 Control Bus

- The 8085 microprocessor uses the control bus to provide the timing signals.
- The microprocessor sends signals on the control bus to enable the outputs of addressed memory devices or I/O port devices.
- Some of the control bus signals are follows :
  (1) Memory read. (2) Memory write.
  (3) I/O read. (4) I/O write.
- These signals are used to identify a device type with which the microprocessor intends to communicate.

2.6 Supporting Circuits

The supporting circuits include the circuits like clock circuit, reset circuit, circuitry required for the generation of control circuits, etc.

2.6.1 Oscillator Circuit

8085 provides ON CHIP OSCILLATOR. Refer Fig. 2.6.1 which shows the internal block diagram of the on chip clock generator.

- It requires tuned circuit e.g. LC, RC, crystal or an external clock source in order to generate clock.
- The JK flipflop divides the frequency by 2. Hence the operating frequency of 8085 is always half of the oscillator frequency.

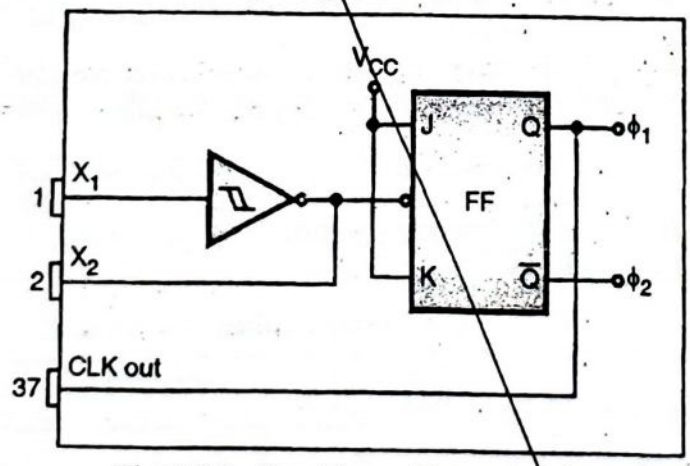

Fig. 2.6.1 : On chip oscillator circuit

Crystal Circuit :

- Fig. 2.6.2 shows crystal interfaced to pin no. 1 and 2. Crystal should be used, when we want stable frequency. Normally, body of crystal is grounded; this avoids external noise interference. Capacitor C_1 / C_2 ; in the range of 10 – 20 pF; is suggested by manufacturer for start up purpose.
- In industry, people use quartz crystal ONLY for clock generation. Crystal determines frequency of oscillation.