7.12 RAM (RANDOM ACCESS MEMORY)

As memory is required for storage of information in digital form. Hence, it plays a vital role in sequential circuits. Memory can be magnetic type which was used earlier or based on semiconductor technology used recently.

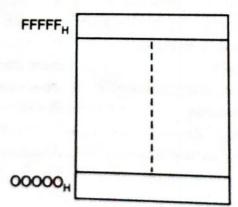
Semiconductor memories are most popular because of their

- · small size
- · low cost
- · high reliability
- High speed of operation and
- Flexibility of expanding size

Memory can be sequentially accessed or random accessed. In sequential accessed memories, each memory location can be accessed in a sequential manner. It means we can't directly go to the desired location for accessing information in terms of reading and writing, limitation involved in case of sequential accessed memory is that access time required for each for each location is different, because each memory location can be accessed in a sequential manner.

In case of RAM, access time required for each location is same. It means, any information can be randomly accessed by just knowing row and column that intersects at memory cell.

Memory is supposed as big array of data and can be seen like this-



This array of data is representing address in the range from $00000_{\rm H}$ - FFFFF₄. This is indicating 20 bit address bus handling $2^{20} = 1 \rm M$ byte memory locations. Purpose of RAM is to temporarily hold programs and data for processing. RAM is said to be volatile because RAM holds, its data as long as computer is switched on. All data in RAM is lost when power is switched off. Before the power is turned off, the binary information from RAM is transferred to disk so that stored information can be retained.

Let's draw a block diagram of RAM

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2^k

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2

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Address Data $2^{\kappa} \times n$ Memory CS -RD . WR .

Specification of RAM: Number of words it contains X capacity of each

- word. • Number of words contained by RAM = 2k
 - Number of bits in each word = n
 - Number of address lines = k

Memory communicates with the external word by means of some lines called as buses. Bus can be address bus, data bus or control bus.

 $2^k \times n$ memory specifies

- k Address Lines
 - ⇒ required to access a particular memory location for reading or writing.
- n Data input lines
 - ⇒ required to store information in the memory
- n data output lines
 - ⇒ required to retrieve information from memory
- $\overline{RD}/\overline{WR}$ control lines

⇒ required to specify direction of transfer for Read access/Write access. Read access is done for retrival of some information from memory and Write access is done to write something into memory.

How to do the read and write access

How to do the read and with		Write access	
	Read access	1	Put address on address lines
1.	Put address on address lines indicating memory location to be accessed	1.	indicating memory location to be accessed for writing.
_	for reading	2.	Put data on data line that mu
2.	Activate \overline{RD} signal	2.	be stored at selected memory
		3.	Activate WR signal

RAM can be classified in two categories:

- 1. Static RAM (SRAM)
- 2. Dynamic RAM (DRAM)

It consists of latches. Latches are used to store binary information. 1. Static RAM

SRAM is easier to use and provides shorter \overline{RD} and \overline{WR} cycles.

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Dynamic RAM

It stores the binary information in the form of electric charges on capacitors are leaky and stored charge. It stores the binary information are leaky and stored charge tends provided inside the chip. These capacitors are leaky and stored charge tends provided inside the chip. Hence, they need periodic refreshing. to decay with time. Hence, they need periodic refreshing.

SUMMARY

- PLDs are those devices in which large circuit is designed on single chip.
- Advantages of PLD's are
 - Reduced power requirements
 - Design security
 - Compact circuitary
 - Short design cycle
 - Low development cost
- PLDs are classified as
 - ROM
 - PLA
 - PAL
 - FPGA
 - CPLDs
- In ROM, AND array is fixed and OR array is programmable.
- In PLA both AND & OR array is programmable.
- In PAL, AND array is programmable and OR array is fixed.
- ROM is denoted by $2^n \times m$ where n is the input variable and m is the output line.
- ROM implementation of a frequation may become quite expensive for function with a large number of variables.
- In PLA, decoder of ROM is replaced with an AND array that perform product terms of the input variables.
- PAL is cheap as compared to PLA.
- FPGAs support thousands of gates. They are especially used for integrated circuit designs.
- FPGAs consists of logic blocks and programmable interconnects.
- CPLD comparies multiple circuit blocks on a single chip, with internal wiring resources to connect the circuit blocks.
- CPLDs range in size from only 2-PAL line blocks to more than 100 PAL-like blocks.
- RAM are of two types (i) static RAM (ii) Dynamic RAM

REVIEW QUESTIONS

- 1. Explain the merits of using PLDs.
- Explain the structure of ROM. 2.
- Design the circuit of full adder using ROM. 3.
- What is the difference between PAL and PLA? 4.
- Design the circuit of Half adder using PAL and PLA. 5.
- Draw and explain the structure of PAL.

programmable L Explain the

- Explain the 7.
- (i) FPGA
 - (ii) CPLD Compare F
- 10. Design the
- 11. Realize the
- 12. Design the
- 13. Write shor
 - (i) ROM (ii) CPLI
- 14. Design th $y = \sum m (0)$
- 15. Design th

gogrammable Logic Devices gic and Design gxplain the structure of PLA. Explain the following on capacitors (i) FPGA charge tends (ii) CPLD Compare FPGA and CPLD. Design the circuit of full subtractor using PAL and PLA. $f = \sum_{n=1}^{\infty} f(n) \int_{-\infty}^{\infty} e^{-int} dt$ Realize the function $f = \Sigma m(0, 1, 2, 3)$ by ROM. pesign the circuit for half subtractor using PAL. ingle chip. Write short note on (i) ROM as PLD (ii) CPLD advantages over FPGA Design the following function using PLA: $y = \sum m (0, 1, 2, 4, 5)$ Design the circuit of full adder using ROM.

output line.
function with

grated circuit

ernal wiring

L-like blocks.