Designing of Excess-3 to BCD Code using PAL

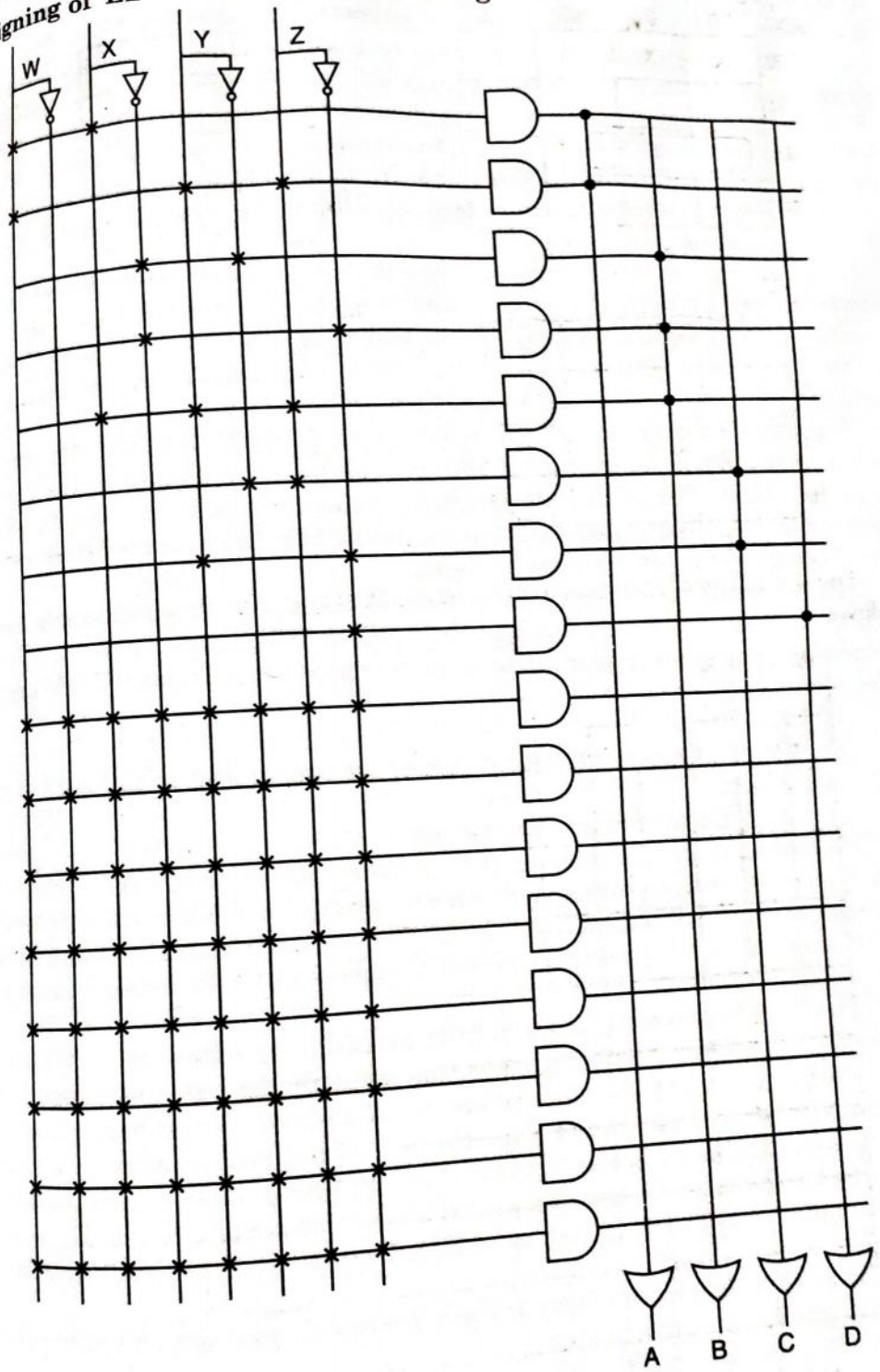

Fig. 7.29.

7.10 FPGA (FIELD PROGRAMMABLE GATE ARRAY)

It is a type of logic chip that can be programmed. An FPGA is similar to a PLD, but whereas PLDs are generally limited to hundred of gates, FPGAs support

thousands of gates. They are especially used for integrated circuit designs. Once the design is set, hardwired chips are produced for faster performance.

A Field programmable gate array is a semiconductor device containing programmable logic components called "logic blocks" and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, XOR or more complex combinational functions such as decoders or mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer, somewhat like a one-chip programmable breadboard. Logic blocks and interconnects can be programmed by the customer or designer, after the FPGA is manufactured, to implement any logical functions hence the name "field programmable".

To configure (program) an FGPA you specify how you want the chip to work with a logic circuit diagram or a source code using a hardware description language (HDL). The HDL form might be easier to work with when handling large structures because its possible to just specify them numerically rather than having to draw every piece by hand.

FPGAs are quite different from CPLDs (Complex Programmable Logic Device) because FPGAs do not contain AND or OR planes. Instead, FPGAs provide logic blocks for implementation of the required functions. FPGA contain three main types of resources :

(1) Logic Blocks
(2) Input/Output–Input/output blocks for connecting to the pins of the package.
(3) Interconnection wires and switches.

The logic blocks are arranged in a two-dimensional array, and the interconnection wires are organized as horizontal and vertical routing channels between rows and columns of logic blocks. The routing channels contain wires and programmable switches that allows the logic blocks to be interconnected in many ways.

Figure 7.20 show two locations for programmable switches, the brown boxes adjacent to logic blocks holds switches that connect the logic block input and output terminals to the interconnection wires and the brown boxes that are diagonally between logic blocks connects one interonnection wire to another (such as a vertical wire to a horizontal wire). Programmable connections also exist between the Input/Output blocks and the interconnection wires. The actual programmable switches and wires in an FPGA varies in commercially available chips.

FPGAs can be used to implement logic circuits of more than a few hundred thousand equivalent gates in size.

Each logic block in an FPGA has a small number of inputs and one output. A number of FPGA products are on the market, featuring different types of logic blocks. The most commonly used logic block is a look up table (LUT), which contains storage cells that are used to implement a small logic function. Each cell is capable of holding a single logic value, either 0 or 1. The stored value is produced as the output of the storage cells. LUTs of various sizes may be created, where the size is defined by the number of inputs.

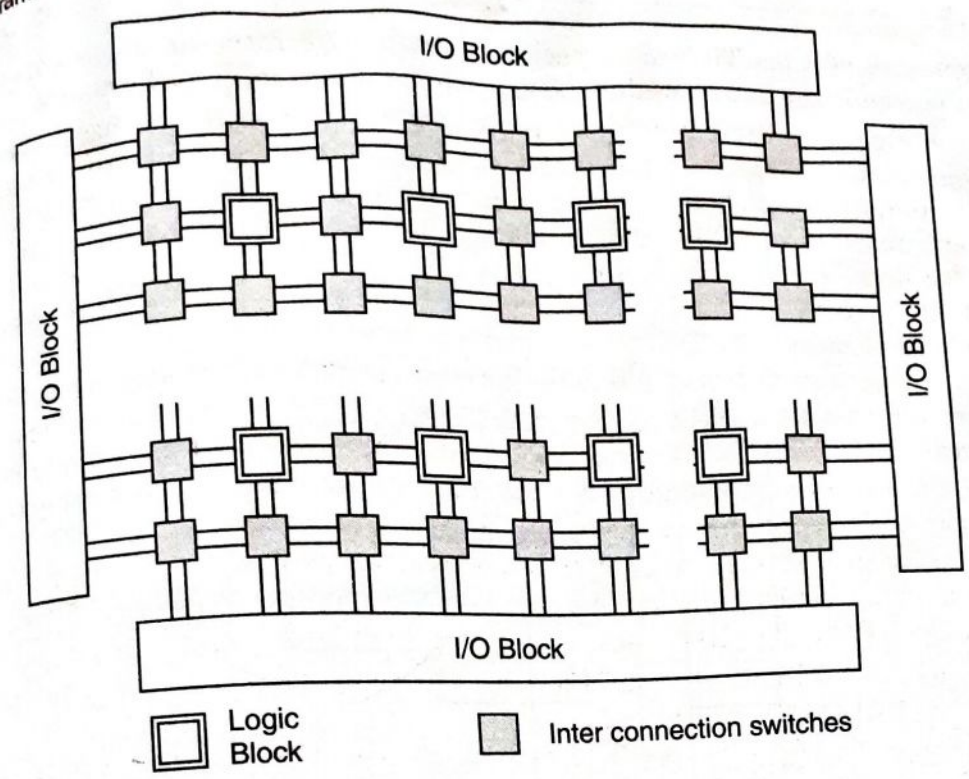

Fig. 7.30. FPGA

Figure 7.21 shows the structure of a small LUT. It has two inputs x_1 and x_2 and one output function f. It is capable of implementing any logic function of two variables. Because a two-variable truth-table has four rows, this LUT has four storage cells. One cell corresponds to the output value in each row of truth table. The input variables x_1 and x_2 are used as the select input of three multiplexers, which, depending on the valuation of x_1 and x_2, select two content of one of the four storage cells as the output of LUT. To realized a logic function by using the two-input LUT, consider the truth-table in fig. 7.22. The function f_1 from this table can be stored in LUT (as 1001 to first input to MUX 1 and 0 to 2nd MUX 1 input and so on). The arrangement of multiplexers in the LUT correctly realizes the functions f_1 when $x_1 = x_2 = 0$, the output of the LUT is

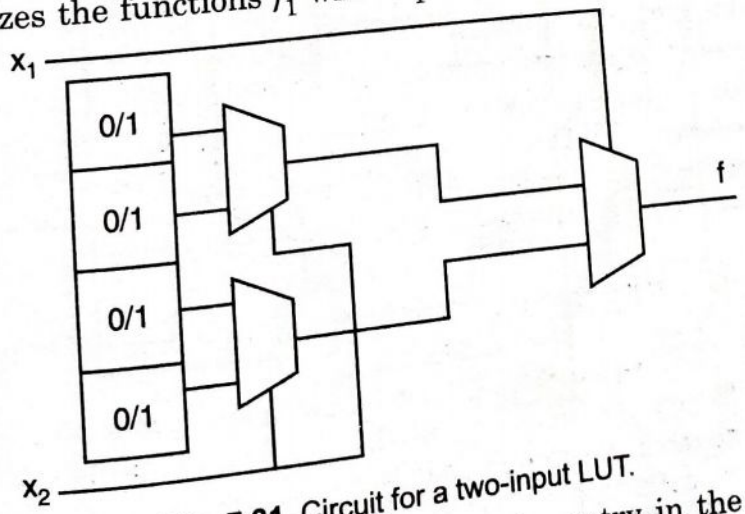

Fig. 7.31. Circuit for a two-input LUT.

driven by the top storage which represents the entry in the truth table for $x_1 x_2 = 00$. Similarly, for all valuations of x_1 and x_2, the logic value stored in the

storage cell corresponding to the entry in the truth table chosen by the particular valuation appears on the LUT output. Providing access to the contents of storage cells is only way in which multiplexers can be used to implement logic functions.

x_1	x_2	y_1
0	0	1
0	1	0
1	0	0
1	1	1

Fig. 7.32. $f_1 = \overline{x_1} \cdot \overline{x_2} + x_1 x_2$

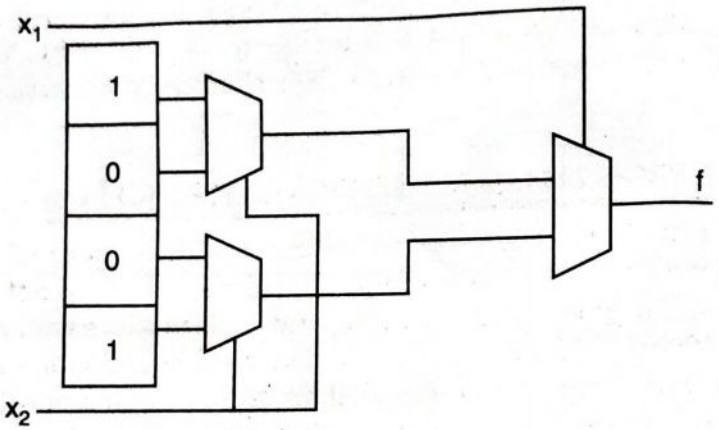

Fig. 7.33. Storage cell contents in the LUT Two-input LUT.

The three input LUT is shown in fig. 7.23. It has eight storage cells because a three-variable truth-table has eight rows.

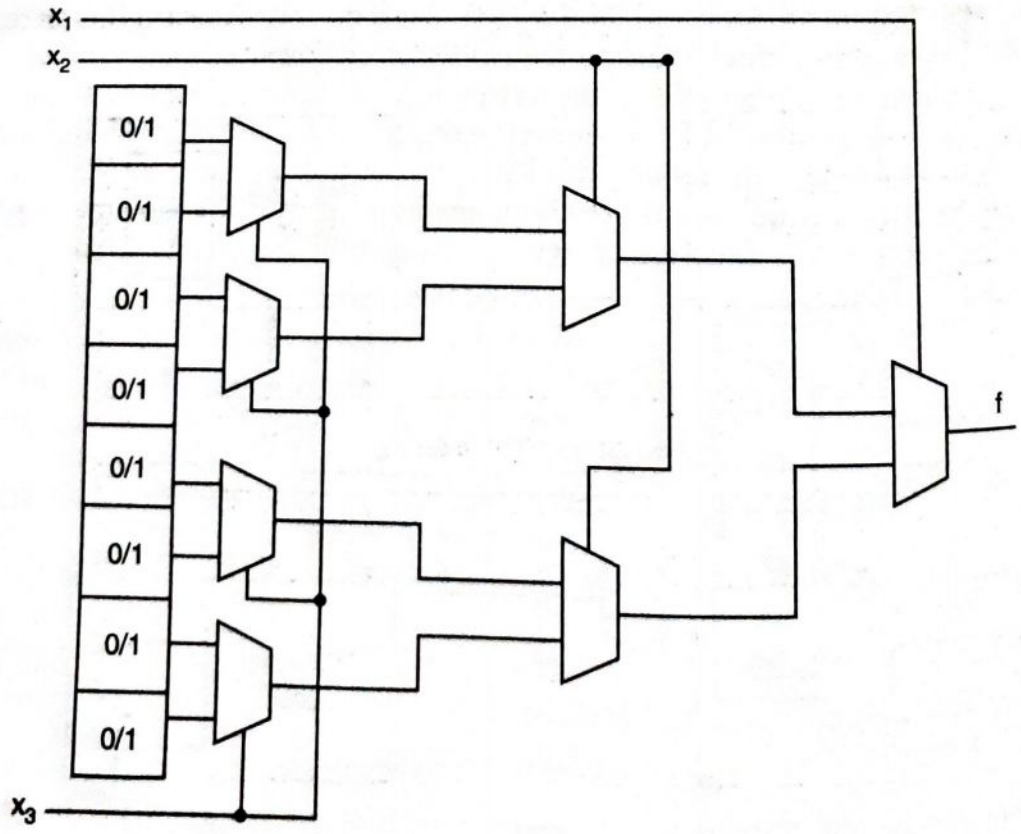

Fig. 7.34. A 3-input LUT

The storage cells in the LUTs in an FPGA are volatile, which means that they lost their stored contents whenever the power supply for the chip is turned off. Hence FPGA has to programmed every time power is applied.

Advantages of FPGA

(1) It is used to design large logic circuits.

(2) It is used to implement logic circuits of more than a few hundred thousand equivalent gates in size.

Demerits of FPGA

The storage cells in the LUTs in an FPGA are volatile. Due to this FPGA has to be programmed every time power is applied. Often a small memory chip that holds its data permanently, called a programmable read only memory (PROM), is included on the circuit board that houses the FPGA. The storage cells in the FPGA are loaded automatically from the PROM when power is applied to the chips.

7.11 COMPLEX PROGRAMMABLE LOGIC DEVICES (CPLDs)

PLAs and PALs are useful for implementing a wide variety of small digital circuits. Each device can be used to implement circuits that do not require more than the number of inputs, product terms, and outputs that are provided in the particular chip. These chips are limited to modern sizes, supporting a combined number of inputs plus outputs of not more than 32. For implementation of circuits that require more inputs and outputs, either multiple PLAs or PALs can be employed or else a more sophisticated type of chip, called a complex programmable logic device (CPLD) can be used.

A CPLD comprises multiple circuit blocks an a single chip, with internal wiring resources to connect the circuit blocks. Each circuit block is similar to a PLA or a PLA. The structure for CPLD is shown as follows :

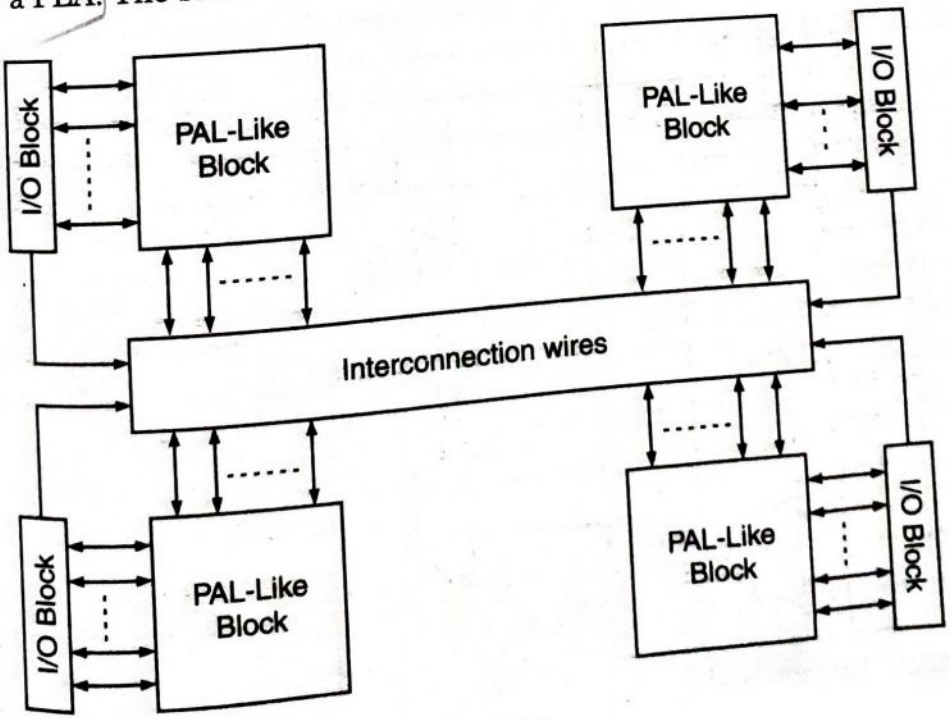

Fig. 7.35.

Structure of CPLD

It includes four PAL – like blocks that are connected to a set of interconnection wires. Each PAL – like block is also connected to a subcircuit labeled Input/Output block which is attached to a number of chips input and output pins.

The PAL like block includes 3 macro cells, each consisting of a four–input OR gate (real CPLDs provides between 5 and 20 inputs to each OR gate).

The OR-gate output is connected to another type of logic gate that we have not yet introduced. It is called an Exclusive–OR (XOR) gate. The behaviour of an XOR gate is the same as per an OR gate except that if both of the inputs are 1, the XOR gate produces a 0. One input to the XOR gate can be programmably connected to 1 or 0, if 1, then the XOR gate complements the OR-gate output and if 0, then the XOR gate has no effect. In some cases XOR gate is connected to macrocell. The macrocell also includes a flip-flop, a multiplexer and a tri-state buffer. The flip-flop is used to store the output value produced by the OR gate. Each tri-state buffer is connected to a pin on the CPLD package. The tri-state buffer acts as a switch that allows each pin to be used either as an output from the CPLD or as an input. To use a pin as an output, the corresponding tri-state buffer is enabled, acting as a switch that is turned on. If the pin is to be used as an input, then the tri-state buffer is disabled, acting as a switch that is turned off. In this case an external source can drive a signal on to the pin, which can be connected to other macrocells using the interconnection wiring. The interconnection wiring contains programmable switches that are used to connect the PAL-like blocks. Each of the horizontal wires can be connected to some of the vertical wires that is crosses, but not to all of them. The number of switches (for connection b/w wires) is chosen to provide sufficient flexibility for typical circuits without wasting many switches.

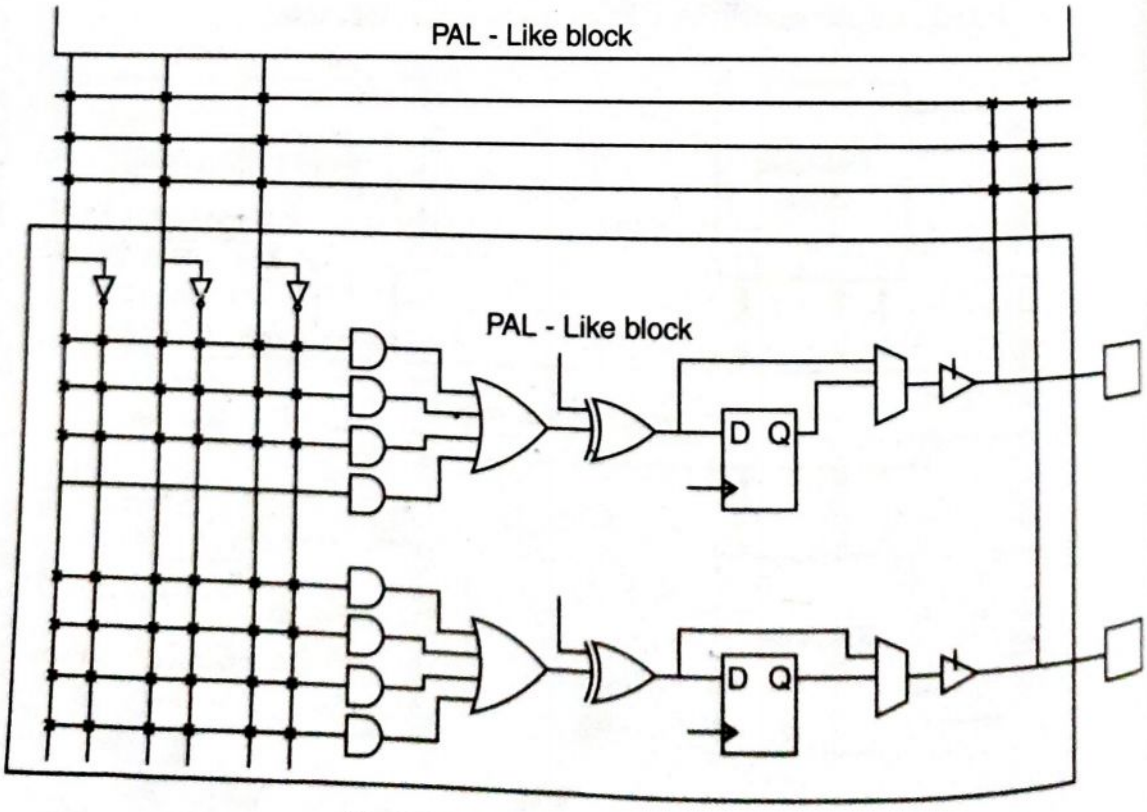

Fig. 7.36. Internal Structure of CPLD.

Commercial CPLDs range is size from only 2 PAL–like blocks to more that 100 PAL–like blocks. Once a CPLD is programmed, it retains the programmed state permanently, even when the power supply for the chip is turned off. This is known as non-volatile programming.

CPLDs are used for the implementation of many types of digital circuits.

The example of certain CPLD product company and its product are as follows–

Manufacture	CPLD Product
Atmel	ATF, ATV
Cypers	FLASH 370, Ultra 37000
Altera	MAX 5000, 7000, 9000

The mostly used CPLD is MAX 7000 which range is size from 7032, has 32 macrocells, to the 7512 has 512 macrocells.

Comparison between FPGA and CPLD

	CPLD	FPGA
(1) Gate capacity	In CPLD gate capacity is 300 – 6,000	In FPGA gate capacity is 800 – 1,00,000 gates
(2) No. of Input/ Outputs	In CPLD it is 30 – 200	In FPGA it is 100 – 5,500 Input/ Input/Outputs.
(3) Process Technology	FROM, EFROM and Flash.	SRAM, Antifuse, EEPROM
(4) Performance	Predictable timing upto 200 MHz today	Application dependent upto 100 MHz today.
(5) Power consumption	0.5 – 2.0 W static 0.5 – 4.0 W dynamic (high)	Very low static Dynamic consumption dependent typical (0.1 – 2W medium value).
(6) Speed	Fast and predicatable	Application dependent.
(7) Interconnect	Crossbar	Routing.
(8) Architecture	PAL – like	Gate array like.
(9) Density	Low to medium	Medium to high.
(10) Area of use	Used for small projects	Used for big project because of large number of large element.
(11) Type of inbuild component	ON-chip RAM, ROM is not present. It is not generally present.	RAM, ROM, counters, shift register is present inbuild.
(12) Flexibility	Lesser as compared to FPGA	More flexibility
(13) When power supply is ON	CPLD starts working as soon as power is switched ON	Takes few micro second to start working.
(14) Complexibility	Less complex	More complex.
(15) Applications	Bus interfaces, wide decreases, fast memory interface.	Simple state machine, complex controllers.