(3) N-bit counter type ADC (Digital ramp type ADC)

Counter type A/D converter circuit consists of following blocks:

(1) Comparator with variable reference voltage

(2) N-bit sequence up counter

(3) N-bit D/A converter

(4) S-R Flip-Flop

(5) AND Gate

Block Diagram of an N-bit counter type ADC:

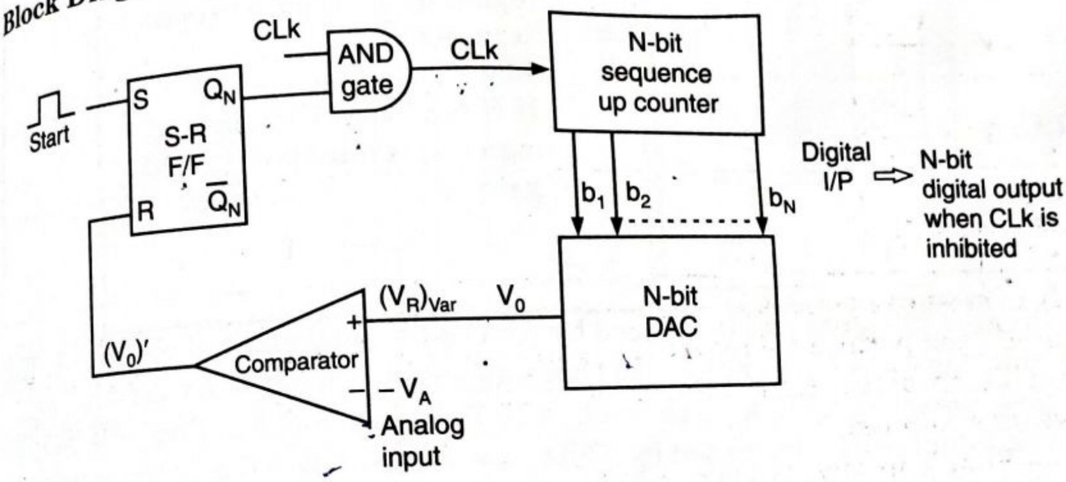


Fig. 6.29.

Operation

Initially counter is reset to zero. It means counter is initialized with value i.e., 0 0 0 0.

Let's say 4 bit counter type ADC, we are going to discuss here. Hence, we require 4-bit sequence up counter and output of counter will be:

b_1	b_2	b_3	b_4	:	0	0	0	0

Now 0 0 0 0 is send to 4-bit DAC and it produces 0 analog voltage by taking equation:

$$V_0 = k\, V_{Ref}\left[b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8}\right]$$

As $\quad b_1 = b_2 = b_3 = b_4 = 0$

Hence, $\quad V_0 = 0\text{ V}$

It means variable reference voltage is equal to 0V.

How comparator works

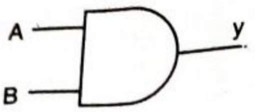
If $V_A > (V_R)_{Var}$
Then $(V_0)' = 0$
Else if $V_A \le (V_R)_{Var}$
Then $(V_0)' = 1$

Obviously if $(V_R)_{Var} = 0\text{V}$, Then $V_A > (V_R)_{Var}$ and hence $(V_0)' = 0\text{V}$.

Now $(V_0)'$ is connected to reset input of S-R flip-flop.

When we apply start pulse to set input of S-R flip-flop, then $S = 1$ and $R = 0$ and S-R Flip-Flop is said to be in set state.

How AND gate works



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

If $B = 1$ Then $Y = A$ means signal by AND gate to output terminal.
Else
If $B = 0$, Then $Y = 0$ means signal A is inhibited by AND gate

Hence, Clk signal will be passed by AND gate until and unless $Q_N = 1$. This will continue until $V_A > (V_R)_{Var}$. In this way counter will progress counting.

Now, when $V_A \leq (V_R)_{Var}$, then $Q_N = 0$. It means S-R flip-flop will be reset and Clk signal will be inhibited by AND gate, means Clk = 0 and counter action will stop means counter stops counting.

In this way conversion is complete and number stored in N-bit sequence up counter is equivalent to N-bit digital data corresponding to provided analog input voltage.

VA	b_1 b_2 b_3 b_4	V_0	$(V_R)_{Var}$	V_0'		S R		Q_N	CLK	Counter
9V	0 0 0 0	0 V	0 V	0 V		1 0	(set)	1	Passed	Progress
	0 0 0 1	1 V	1 V	0 V		0 0		1	Passed	Progress
	0 0 1 0	2 V	2 V	0 V		0 0		1	Passed	Progress
	0 0 1 1	3 V	3 V	0 V		0 0		1	Passed	Progress
	0 1 0 0	4 V	4 V	0 V	$V_A >$	0 0	No change	1	Passed	Progress
	0 1 0 1	5 V	5 V	0 V	$(V_R)_{Var}$	0 0		1	Passed	Progress
	0 1 1 0	6 V	6 V	0 V		0 0		1	Passed	Progress
	0 1 1 1	7 V	7 V	0 V		0 0		1	Passed	Progress
	1 0 0 0	8 V	8 V	0 V		0 0		1	Passed	Progress
	1 0 0 1	9 V	9 V	1 V	$V_A = (V_R)_{Var}$	0 1		0	Inhibited	

Counter stops counting and number stored in counter is 1001 and i.e., final result.

4. Dual Slope A/D Converter

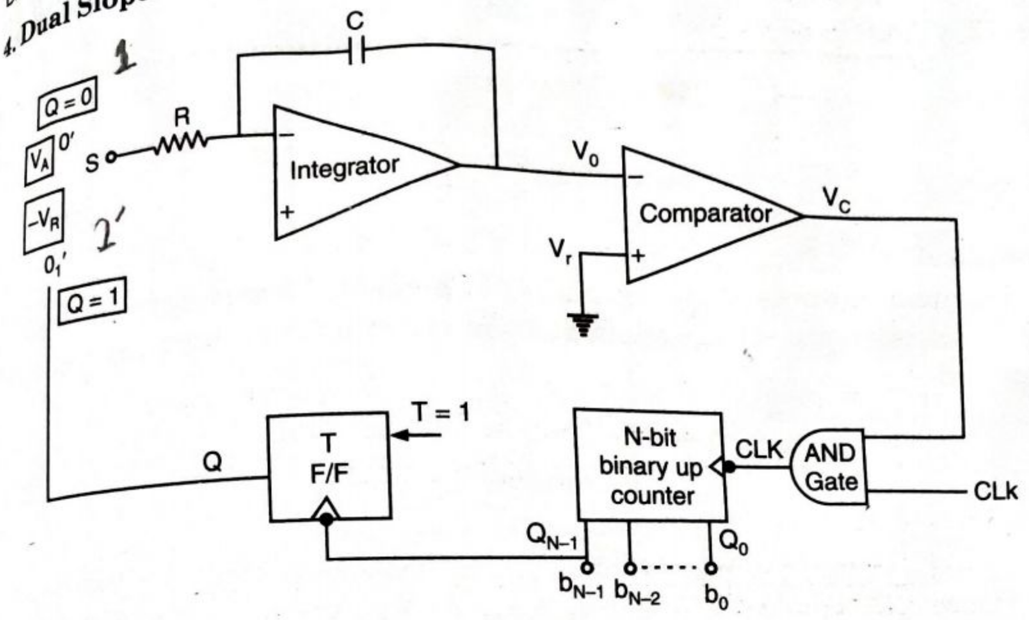


Fig. 6.30. Block Diagram

Complete block diagram consist of following blocks :

(1) SPDT switch (S)
(2) Integrator
(3) Comparator
(4) AND Gate
(5) N-bit binary up counter
(6) T F/F

Working

SPDT switch (S) can be hold in two positions *i.e.*, either 1 (Up position) or 1′ (down position). It depends upon output of T flip-flop (Q). If $Q = 0$, then switch will be pushed upwards. If $Q = 1$, then switch will be pushed in downward direction (1′ position).

As initial state of T flip-Flop is taken as 0 (when no Clk pulse is provided to it), Hence, $Q = 0$. when $Q = 0$, then switch S is pushed in upward position.

Integrator : In this way analog input voltage (V_A) is provided as input to integrator.

In this way—

$$V_0 \text{ (output of integrator)} = \frac{-1}{R_C}\int_0^t V_A\,dt \qquad ((R_C = \tau) \text{ Time constant})$$

$$\Rightarrow \qquad V_0 = \frac{-1}{\tau}\int_0^t V_A\,dt$$

$$\Rightarrow \qquad V_0 = \frac{-1}{\tau}V_A\int_0^t dt$$

$$\Rightarrow \quad V_0 = \frac{-1}{\tau} V_A [t]_0^t$$

$$\Rightarrow \quad V_0 = \frac{-1}{\tau} V_A [t - 0]$$

$$\Rightarrow \quad V_0 = \frac{-V_A}{\tau} t$$

Comparator:

Comparator works on two inputs *i.e.*, V_0 applied at inverting input terminal and V_r *i.e.*, reference voltage applied at non inverting input terminal connected to ground.

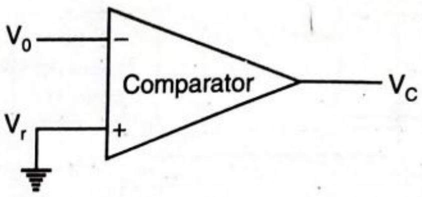


Fig. 6.31.

In comparator, we see that:

If $V_0 > 0$, then $V_C = 0$. It means if V_0 obtained is +Ve, then V_C obtained is low.

Else if $V_0 < 0$, then $V_C = 1$. It means if V_0 obtained is – Ve, then V_C obtained is high.

From output of integrator *i.e.*, $V_0 = \frac{-V_A}{\tau} t$, we can see that: As $V_0 < 0$, Hence $V_C = 1$.

AND Gate:

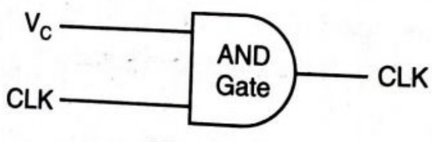


Fig. 6.32.

As $V_C = 1$, hence CLK signal is simply passed by AND gate at its output terminal.

N-bit binary up counter:

Initially counter is reset *i.e.*, $b_2\, b_1\, b_0 = 000$. As we have assumed 3 bit binary up counter. Hence three output terminals are taken as $b_2\, b_1\, b_0$. As CLK signal (output of AND gate) reaches the CLK input of 3-bit counter. In this way counter

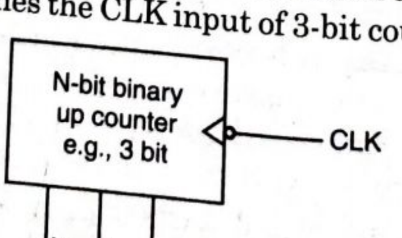


Fig. 6.33.

progresses and incremented by 1 *i.e.*, $b_2\, b_1\, b_0 = 001$. Counter will keep on counting from 0 0 0 to 1 1 1 and takes 7 CLK pulses. At 8[th] CLK pulse, counter is again cleared. By table drawn below, we can observe how counter does progress:

CLK	b_2	b_1	b_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0 recyles

As counter takes a transition from 111 to 000, then b_2 takes a transition from 1 to 0, and this 1 – 0 transition is acting as a CLK pulse of T flip-flop. As T flip-flop is – Ve edge triggered, hence it toggles on – Ve edge of CLK (i.e., 1 – 0 transition of b_2). In this way initial Q which was 0 is now set to 1.

As Q becomes 1 and hence switch S takes a transition from upper position to lower position i.e.1' position. It takes t_1 time to progress counter from 000–111 and then recycle again to 000.

At t_1 instant, V_R is connected to integrator.

$$V_0 = \frac{-1}{\tau}\int_0^t V\, dt$$

where V is taken as generalized input passed by switch (S) to integrator.

$$V_0 = \frac{-1}{\tau}\left[\int_0^{t_1} V_A dt + \int_{t_1}^{t} (-V_R) dt\right]$$

$$V_0 = \frac{-1}{\tau}\left[V_A (t)_0^{t_1} + (-V_R)(t)_{t_1}^{t}\right]$$

$$\Rightarrow \qquad V_0 = \frac{-1}{\tau}\left[V_A(t_1) - V_R(t - t_1)\right]$$

$$\Rightarrow \qquad V_0 = \frac{-1}{\tau} V_A\, t_1 + \frac{V_R}{\tau}(t - t_1)$$

As negative output of integrator is now added with some + Ve value. Hence output of integrator now starts to move in positive direction. But ultimately V_0 remains – Ve and output of comparator *i.e.*, $V_C = 1$ and hence CLK signal will be passed by AND gate and counter will keep on doing progress.

At t_2 instant, V_0 becomes zero and starts to go in positive direction. As soon as V_0 becomes positive. Now output of comparator becomes 0 and in this way CLK signal will be inhibited by AND gate.

Finally counter will stop counting, as it is enable to get CLK pulses.

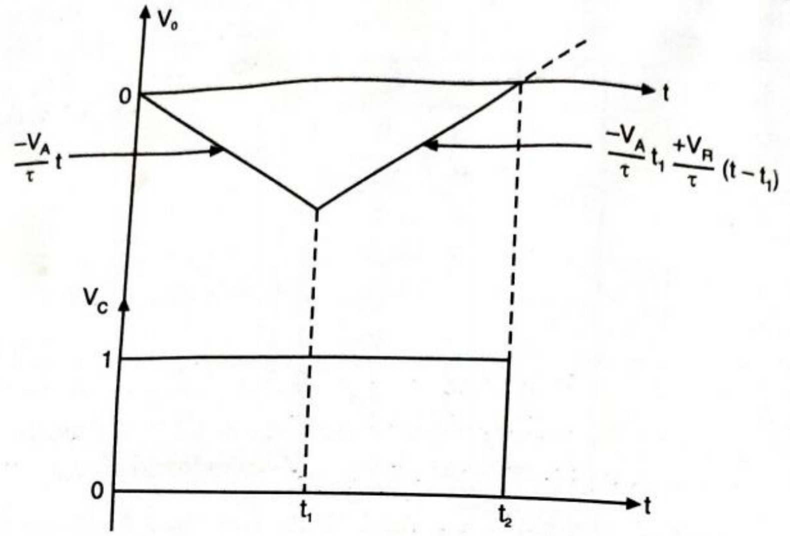


Fig. 6.34.

It we observe the CLK pulses corresponding to progress of counter, we see that

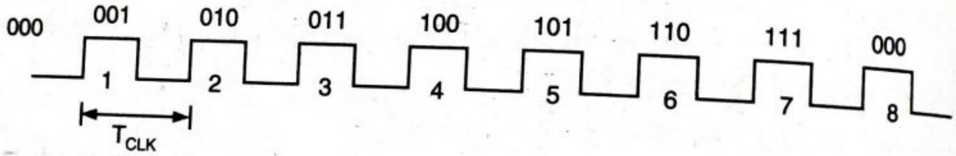


Fig. 6.35.

Total 8 CLK pulses are required to progress a counter from 001 to back 000. Time period of a single CLK pulse is assumed as T_{CLK}. So total time consumed by 8 CLK pulses is 8 T_{CLK}. This total time, we have assumed is t_1.

In this way

$$t_1 = 8\ T_{CLK}$$

For N-bit binary up counter, t_1 is given as :

$$t_1 = 2^N\ T_{CLK}$$

After t_1 time, output of integrator is given as

$$V_0 = \frac{-V_A}{\tau} t_1 + \frac{V_R}{\tau}(t - t_1) \qquad [V_0 = 0]_{t=t_2}$$

$$\Rightarrow \quad 0 = \frac{-V_A}{\tau} t_1 + \frac{V_R}{\tau}(t_2 - t_1)$$

$$\Rightarrow \quad \frac{V_R}{\tau}(t_2 - t_1) = \frac{V_A}{\tau} t_1$$

$$\Rightarrow \quad \frac{V_R}{\tau} t_2 - \frac{V_R}{\tau} t_1 = \frac{V_A}{\tau} t_1$$

$$\Rightarrow \quad \frac{V_R}{\tau}(t_2 - t_1) = \frac{V_A}{\tau} t_1$$

$$t_2 - t_1 = \frac{V_A}{V_R} t_1$$

$\Rightarrow$

$$t_2 - t_1 = \frac{V_A}{V_R} 2^n T_{CLK}$$ [Assume $t_2 - t_1 = nT_{CLK}$ where n is output of counter at t_2]

$\Rightarrow$

$$n\, T_{CLK} = \frac{V_A}{V_R} 2^n T_{CLK}$$

$\Rightarrow$

$$n = \frac{V_A}{V_R} 2^n$$

$\Rightarrow$

$$n = V_A \big|_{V_R = 2^n}$$

$\Rightarrow$

From this mathematical result, we observe that, output of counter is proportional to analog input voltage V_A under the condition $V_R = 2^n$.

6.7 SAMPLE AND HOLD CIRCUIT

Sample and hold circuit generally consists of two FET's. One FET is acting as sampling switch and 2nd FET is acting as Discharging switch. It is used to generate flat top PAM. Pulse amplitude modulation is defined as the type of modulation in which amplitudes of rectangular pulses, *i.e.* carrier is varied according to the instantaneous value of the modulating signal. Flat Top PAM is most popular and widely used. The reason for using flat top PAM is that during the transmission, the noise interefers with the top of the transmitted pulses and this noise can be easily removed if the pulses has flat top.

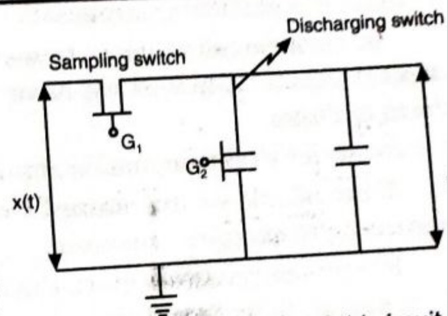


Fig. 6.36. Sample and hold circuit

Working

A sample and hold circuit is shown in Fig. 6.2 is used to produce flat top sampled PAM. The working principle is simple. The sample and Hold (S/H) circuit consists of two field effect transistors (FET) switches and a capacitor. The sampling switch is closed for a short duration by a short pulse applied to the gate G_1 of the transistor. During this period, the capacitor 'C' is quickly charged upto a voltage equal to the instantaneous sample value of the increasing signal $x(t)$. Now, the sampling switch is opened and the capacitor 'C' holds the charge. The discharge switch is then closed by a pulse applied to gate G_2 of the other transistor. Due to this, the capacitor 'C' is discharged to zero volts. The discharge switch is then opened and thus capacitor has no voltage. The waveforms is shown as figure 6.37.

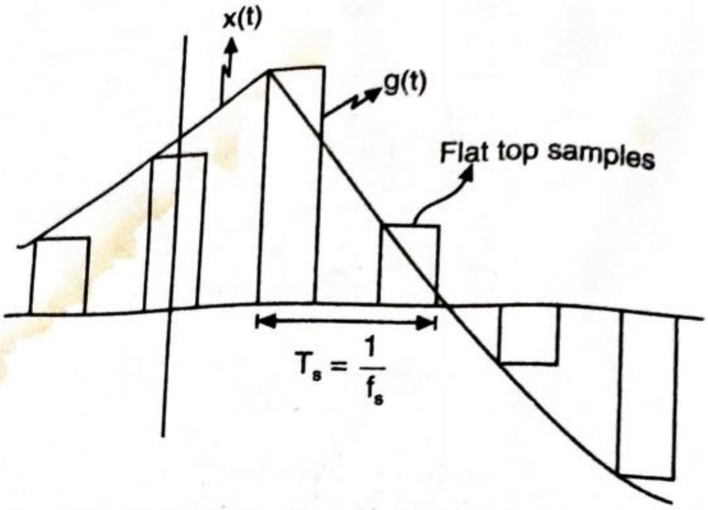


Fig. 6.37. Output waveform of sample and hold circuit

6.8 QUANTIZATION

Sometimes we have an analog signal, however we have to transmit a digital signal for a particular application.

In such cases, we need to convert : An analog signal $\xRightarrow{\text{into}}$ its equivalent digital signal. It means we have to convert: A continuous time signal in the form of digits.

Now, let's take an analog signal—

First of all, we get **sample of this signal** according to sampling theorem.

For this purpose, we mark the time instant t_0, t_1, t_2 and so on at **equal time intervals along x axis** (time axis).

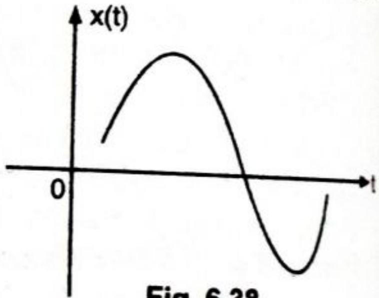


Fig. 6.38.

At each of these time instants, magnitude of signal is measured and thus **samples of signals** are **taken.**

Representation of analog signal an terms of samples in fig. 6.36.

Now, signal is defined only at the sampling instant.

Now, we can say that, the signal is no longer a continuous function of time, but rather its a discrete time signal.

But magnitude of each sample can take any value in a continuous range. Hence signal is still an analog signal.

This difficulty is resolved by a process known as quantization.

In quantization: "**The total amplitude range which the signal may occupy is divided into a number of standard levels**".

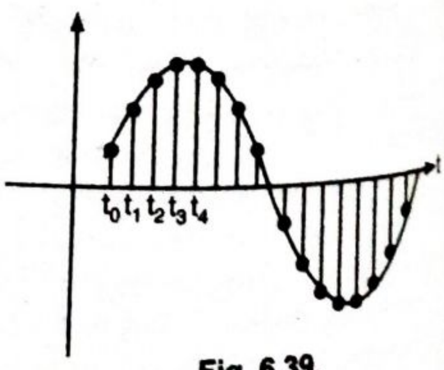


Fig. 6.39.

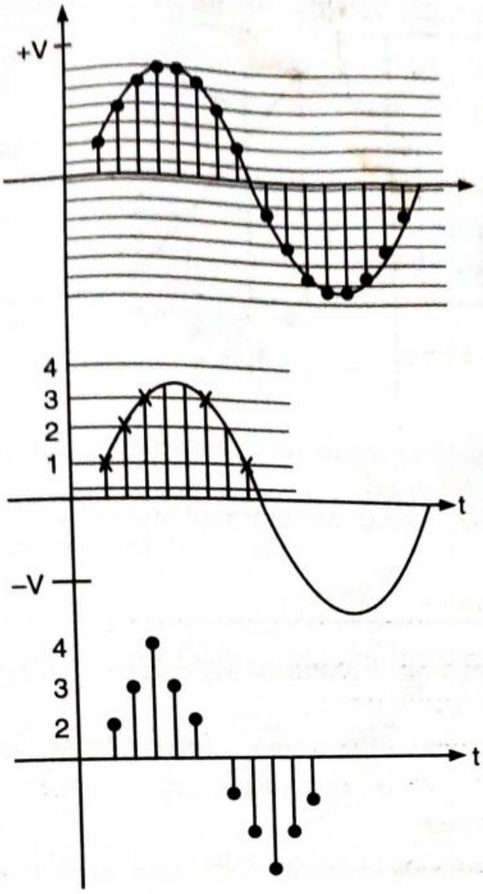


Fig. 6.40.

Amplitudes of signal $x(t)$ lie in the range $(-m_p, m_p)$ which is partitioned into L intervals each of magnitude $\Delta V = \frac{2m_p}{L}$.

Now each sample is approximated or rounded off to the nearest quantized level.

Since each sample is now approximated to one of the L numbers, therefore the information is digitized.

The quantized signal is an approximation of original one.

We can improve the accuracy of quantized signal to any desired degree simply being number of levels L.

$\Delta \rightarrow$ step size

Maximum quantization error will be $\pm \frac{\Delta}{2}$

$$\boxed{\Delta = \frac{m_p - (-m_p)}{L} = \frac{2m_p}{L}}$$

$$\Sigma_{max} = \left|\frac{\Delta}{2}\right|$$

6.9. SPECIFICATIONS OF ADC (GOVERNING CHARACTERISTICS OF ADC)

These characteristics play an important role to determine the performance of ADC. Characteristics are specified as—

(1) Resolution
(2) Input voltage range
(3) Conversion time
(4) Differential linearity
(5) Accuracy
(6) Quantization Error

(1) Resolution

Resolution of an ADC depends on the reference voltage (V_{Ref}) and the number of bits (n) in the digital output.

This is given as

$$\text{Resolution} = \frac{V_{Ref}}{2^n}$$

e.g., 8 bit ADC works on reference voltage 5 V, find out its resolution:

$$= \frac{V_{Ref}}{2^n} = \frac{5\,V}{2^8} = 0.0195 \text{ V} \approx 0.02 \text{ V}$$

(2) Input Voltage Range

It is the range of voltage than an ADC can accept as its input.

(3) Conversion time

The time required by an ADC to convert an analog input value into its equivalent digital data is called as conversion time.

(4) Differential Linearity

It is an important measure of ADC performance. It is defined as a "measure of the variation in voltage step size that causes the converter to change from one state to next". It is normally expressed as a percentage of average step size. Counter type and continuous type ADCs normally have better differential linearity than successive approximation type ADCs.

If step size remains constant throughout the input range, then ADC is said to be linear.

(5) Accuracy

Since both analog and digital systems such as comparator and D/A converters are used for construction of ADC. Hence, overall accuracy of an ADC depends upon both analog and digital systems.

(6) Quantization Error

A digital error in an ADC is based on resolution of digital system. In ADC, a continuous analog voltage is represented by an equivalent set of digital numbers.

When digital numbers are converted back to analog voltage by a DAC, the output is a staircase waveform which is a discontinuous signal compared of a number of discrete steps. The smallest digital step is due to LSb and it can be made smaller only by increasing number of bits in digital representation.

This error is called as quantization error.

The way the register counts is identical to the trial and fit method of decimal to binary conversion whereby different values of bits are tried from MSb to LSb to get a binary number that equals original decimal number.

Conclusion:

4 bit successive approximation type ADC requires 4 conversion cycles. Similarly 8-bit successive type ADC requires 8 conversion cycles. In this way conversion time doesnot depends on amplitude of analog input voltage (for a contant number of bits in digital output).

Advantages

— Reliable
— Capable of high speed
— Lower power consumption
— High regulation and accuracy

Limitation

— Lower sampling rates
&
— Requirements for the building blocks (such as DAC and comparator) to be accurate as overall system.

In successive approximation type ADC, conversion time is constant and proportional to No. of bits in digital o/p unlike counter & continuous type ADC.

SUMMARY

- Data converters are used to convert one form of data to another form of data.
- Digital to analog converter converts digital data into its equivalent analog data. They are used to drive motors.
- Analog to digital converter converts analog data into its equivalent digital data.
- Quantization is a process of appropriating analog signal. It is used in pulse code modulation.
- Resolution is defined as change in output voltage as a fraction of full scale output range.
- Accuracy is predicted as percentage of maximum output voltage.
- Limitation of weighted resistor type DAC is that it requires too many values of resistances.
- Accuracy is measure of effectiveness involved in conversion from analog to equivalent digital signal.
- Successive approximation type A/D converter has the following advantages :
  - Conversion time in constant
  - Conversion time is proportional to number of bits in the digital output.
- Format of Digital output is decided according to need of output which is further interfaced with any other network.
- Range of input voltage is the difference of maximum and minimum analog input voltage which can be applied to *ADC*.