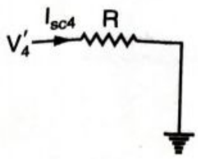


Fig. 6.21.

$$I_{SC4} = \frac{V_4{}'}{R}$$

$$\boxed{I_{SC\,4} = \frac{V_4}{16R}}$$

6.5. ANALOG TO DIGITAL CONVERTER (ADC)

It converts analog data into its equivalent digital data.

Use of digital data: For easy processing.

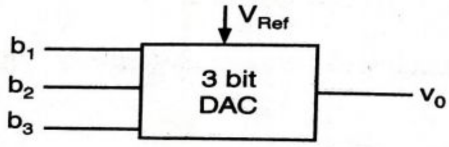


Fig. 6.22.

6.6. CLASSIFICATION OF ADC

ADC can be classified into following categories:

— Successive approximation type ADC
— Simultaneous type ADC
— Counter type ADC
— Dual slope ADC

(1) Successive Approximation Type A/D Converter

It's a type of analog to digital converter that converts a continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.

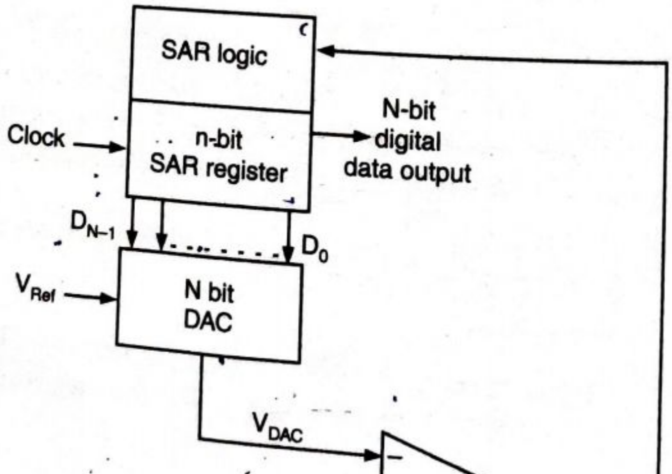


Fig. 6.23.

Circuit consists of—

(1) Sample and hold circuit
(2) Analog voltage comparator
(3) Digital to analog converter
(4) SAR logic

(1) Sample and hold circuit

It acquires the input voltage. It is used to sample analog I/P voltage and hold (i.e., keeping a non changing copy) the sample value whilst binary search is performed.

(2) Analog voltage comparator

It compares input analog voltage (V_{IN}) to output of internal DAC and result of comparison i.e., output of comparator is provided to successive approximation register (SAR).

(3) SAR Logic

It provides on approximate digital code of V_{IN} to internal DAC.

(4) Internal N-bit DAC

It supplies comparator with an analog voltage equivalent of digital code output of SAR.

Analog to digital conversion

The analog input voltage is held on a track/hold. To implement binary search algorithm.

N-bit register is first set to mid scale. e.g., if 8-bit register is there, then that is scaled to – 100.

Else if 16-bit register is there, then that is scaled to 1000.

This forces DAC output to be $\frac{V_{Ref}}{2}$ where V_{Ref} is reference voltage provided to DAC.

A comparison is then performed to determine if

$$V_{IN} > V_{DAC} \text{ or } V_{IN} < V_{DAC}$$

Case 1

If $V_{IN} > V_{DAC}$

Then MSb $\xrightarrow{\text{Retained as}}$ 1

2^{nd} MSb $\xrightarrow{\text{Set to}}$ 1

Case 2

Otherwise if $V_{IN} < V_{DAC}$

Then MSb $\xrightarrow{\text{reset to}}$ 0

2^{nd} MSb $\xrightarrow{\text{Set to}}$ 1

Then SAR control logic moves to next bit-down and again comparison is made so as to decide that MSb is retained or reset. In this way above process is repeated down to LSb. Once this is done, then conversion is complete and N-bit digital word is available in register.

e.g.,—Let's take 4-bit ADC and initially reset SAR i.e., storing value 0000.

$$\boxed{0\,0\,0\,0}$$

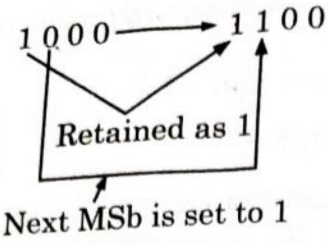
Now, we put MSb = 1, so that reference voltage is set = 8. We are putting it 8, because Maximum combinations will be $2^4 = 16$ and reference is maintained half of that i.e., 1000

$$0000 \rightarrow 1000$$

Now, we need to consider two case—

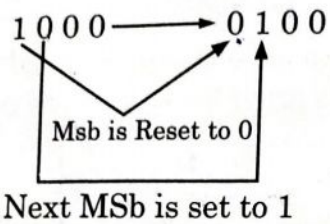
Case 1: If $V_{IN} > V_{DAC}$ $\qquad\qquad$ $V_{IN} \geq V_{DAC}$

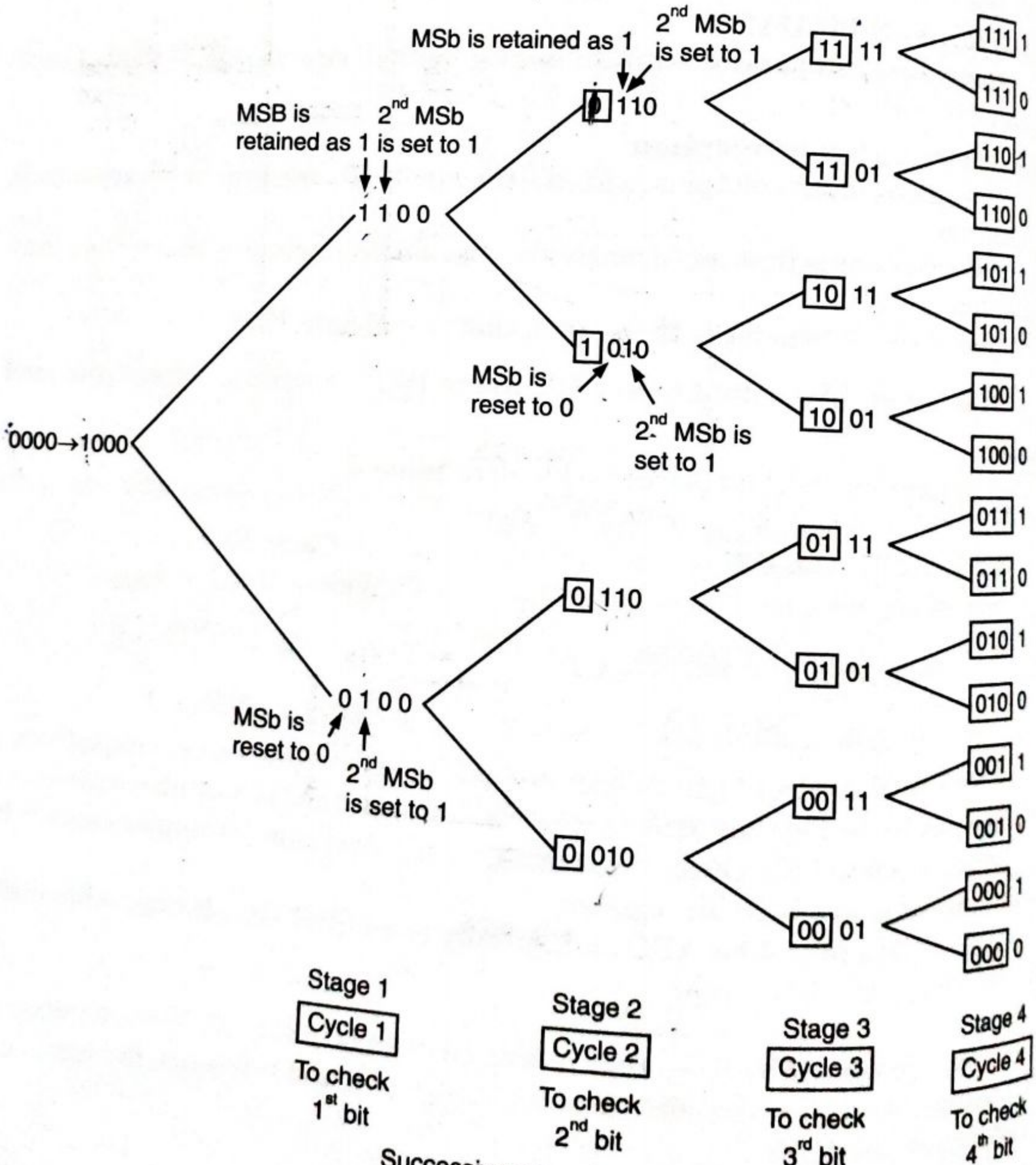
Then



Case 2 : If $V_{IN} < V_{DAC}$ $\qquad\qquad$ $V_{IN} < V_{DAC}$

Then





Successive approximate conversion method

Fig. 6.24.

2. Simultaneous Type A/D Converter (Parallel-Comparator) Flash ADC

This ADC is based on principle that "An unknown analog input voltage is compared with a set of reference voltage"

For N-bit ADC, $2^N - 1$ Comparator are required

e.g., 2 bit ADC $\xrightarrow{\text{Requires}}$ 3 Comparators

$\Rightarrow$ 3 bit ADC $\xrightarrow{\text{Requires}}$ 7 Comparators

$\Rightarrow$ 4 bit ADC $\xrightarrow{\text{Requires}}$ 15 Comparators

Block diagram of 2-bit simultaneous type ADC.

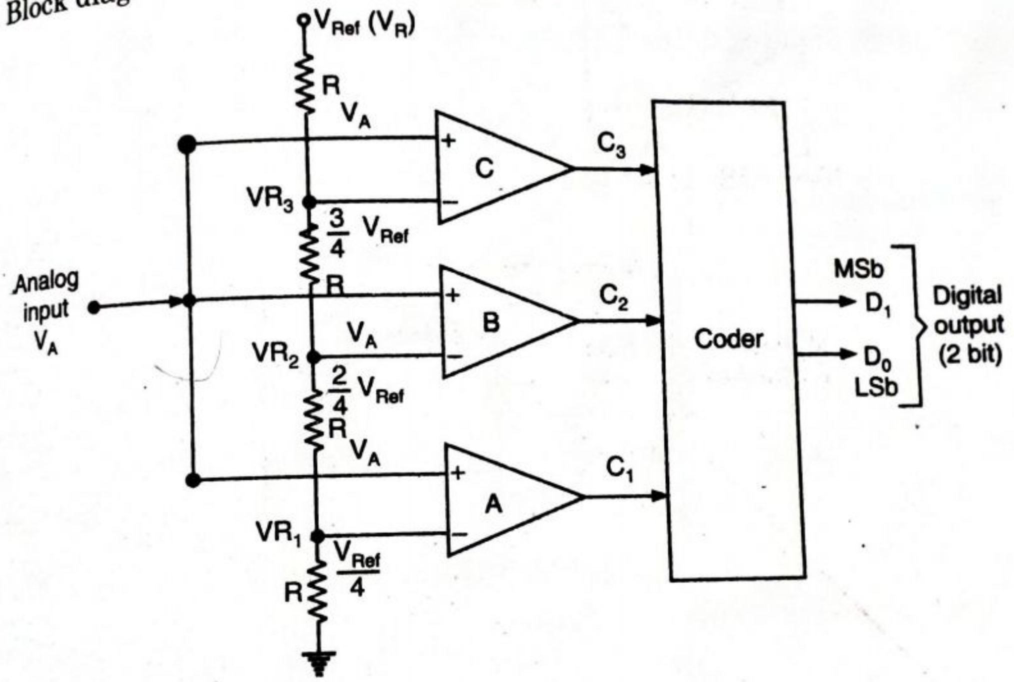


Fig. 6.25.

Let's find values of V_{R1}, V_{R2} and V_{R3}

Determination of V_{R3}

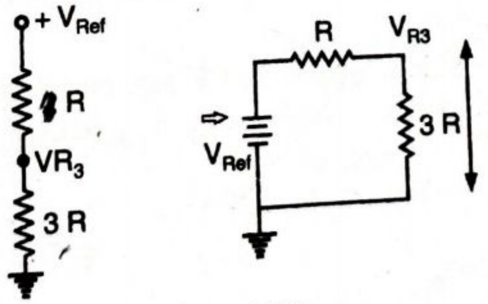


Fig. 6.26.

By voltage dividing rule

$$V_{R3} = \frac{V_{\text{Ref}}(3R)}{R + 3R}$$

$$= \frac{3}{4} V_{\text{Ref}}$$

Determination of V_{R_2}

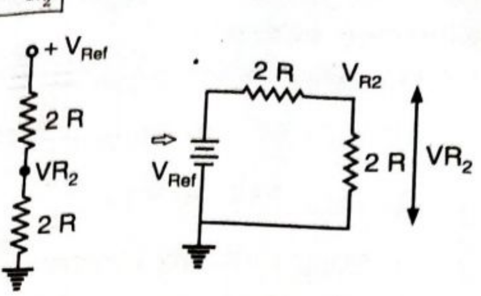


Fig. 6.27.

By voltage dividing rule

$$V_{R_2} = \frac{V_{\text{Ref}}(2R)}{2R + 2R} = \frac{2}{4} V_{\text{Ref}}$$

Determination of V_{R_1}

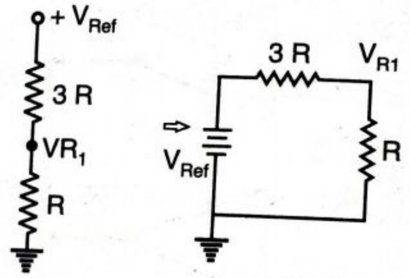


Fig. 6.28.

By voltage dividing rule

$$V_{R_1} = \frac{V_{\text{Ref}}(R)}{R + 3R} = \frac{1}{4} V_{\text{Ref}}$$

Circuit Description—

We have taken 3 OP-AMP acting as 3 comparators A, B, C.

Non inverting inputs of comparators A,B,C are connected to analog input voltage (V_A).

Inverting inputs of comparators A,B,C are connected to a set of reference voltages V_{R_1}, V_{R_2} and V_{R_3} repetitively. V_{R_1}, V_{R_2} and V_{R_3} are determined as—

$$V_{R_1} = \frac{-V_{\text{Ref}}}{4}$$

$$V_{R_2} = \frac{-2V_{\text{Ref}}}{4}$$

$$V_{R_3} = \frac{-3}{4} V_{\text{Ref}}$$

How Comparator Works

If voltage at non inverting input terminal is greater than voltage at inverting terminal, then output of comparator is high.

Else if voltage at inverting input terminal is greater than voltage at non inverting input terminal, than output of comparator is low.

Let's divide the whole analysis in 4 cases—

Case 1: If V_A (analog input voltage) is—

$$\frac{3V_{\text{Ref}}}{4} < V_A \le V_{\text{Ref}}$$

Output of comparator $C = 1$

Hence output of comparator $B = 1$

Similarly output of comparator $A = 1$

$$\boxed{V_A > \frac{3V_{\text{Ref}}}{4} > \frac{2}{4}V_{\text{Ref}} > \frac{V_{\text{Ref}}}{4}}$$

Output of comparator A	Output of comparator B	Output of comparator C
$\Downarrow$	$\Downarrow$	$\Downarrow$
$C1 \Rightarrow 1$	$C2 \Rightarrow 1$	$C3 \Rightarrow 1$

In this way coder provides output as $\boxed{D_1 D_0}$ *i.e.*, digital output of 2 bit equivalent of analog input (V_A).

$$\boxed{\begin{array}{ccc} C_1 & C_2 & C_3 \\ \downarrow & \downarrow & \downarrow \\ 1 & 1 & 1 \end{array}} \longrightarrow \boxed{\begin{array}{cc} D_1 & D_0 \\ \downarrow & \downarrow \\ 1 & 1 \end{array}}$$

As three of the comparators are providing 1, hence output of coder is equivalent of 3 *i.e.*, 11.

Case 2 : If $\dfrac{V_{\text{Ref}}}{2} < V_A \le \dfrac{3V_{\text{Ref}}}{4}$

Hence, Output of comparator $A = 1$

Output of comparator $B = 1$

But Output of comparator $C = 0$

$$\boxed{\begin{array}{l} V_A > \dfrac{V_{\text{Ref}}}{2} > \dfrac{V_{\text{Ref}}}{4} \\ \text{But } V_A < \dfrac{3V_{\text{Ref}}}{4} \end{array}}$$

$$\boxed{\begin{array}{ccc} C_1 & C_2 & C_3 \\ \downarrow & \downarrow & \downarrow \\ 1 & 1 & 0 \end{array}} \longrightarrow \boxed{\begin{array}{cc} D_1 & D_0 \\ 1 & 0 \\ \cancel{0} & \cancel{1} \end{array}}$$

As only one comparator is providing output 1. Hence, output of coder is equivalent of 1 *i.e.*, ~~01.~~ 10

Case 4 : If $0 \le V_A \le \dfrac{V_{\text{Ref}}}{4}$

Hence, Output of comparator $A = 0$

Output of comparator $B = 0$

Output of comparator $C = 0$

$$\boxed{\begin{array}{ccc} C_1 & C_2 & C_3 \\ \downarrow & \downarrow & \downarrow \\ 0 & 0 & 0 \end{array}} \longrightarrow \boxed{\begin{array}{cc} D_1 & D_0 \\ 0 & 0 \end{array}}$$

As no comparator is providing output as 1. Hence, output of coder is equivalent of 0 *i.e.*, 00.

Concluding with the table—

V_A Analog input	Comparator *A* output C_1	Comparator *B* output C_2	Comparator *C* output C_3	D_1 D_0 Digital output
$0 \le V_A \le \frac{V_{Ref}}{4}$	0	0	0	0 0
$\frac{V_{Ref}}{4} < V_A \le \frac{V_{Ref}}{2}$	1	0	0	0 1
$\frac{V_{Ref}}{2} < V_A \le \frac{3V_{Ref}}{4}$	1	1	0	1 0
$\frac{3V_{Ref}}{4} < V_A \le V_{Ref}$	1	1	1	1 1

It is most component intensive for any given no. of output bits. 3 bit ADC requires 7 comparators. 4 bit ADC requires is comparators. For each additional output bit, no. of required comparator doubles. Here, flash methodology quickly shows its weakness.

— Simple in terms of operational theory

— Efficient in terms of speed

— Being limited only in comparator and gate propagation delay. An additional advantage of flash converter often over-looked is ability for it to produce a non linear output. With equal value resistors in reference voltage divider network, each successive binary can't represents same amount of analog signal increase, providing a proportional response.

For specific applications: The resistor values in divider network may be made non equal. This give ADC a custom, non linear response to analog input signal.

No other ADC design is able to grant this signal conditioning behaviour with just a few component value changes.

Advantages

— Simultaneous type ADC is fastest because A/D conversion is performed simultaneously through a set of comparators

$\Downarrow$ Hence

it is also called as a flash type ADC

— The construction is simple and easy to understand

Disadvantages

Simultaneous type ADC is not suitable for ADC with more than 3 or 4 digital output bits.

As 2^n-1 comparators are required for an *n*-bit ADC

Number of comparators required to implement increases very rapidly.