

e.g.,— Let's say final output desirable is 7 V. Hence, output is said to be settled if it lies in the range  $7 \pm 0.5$  i.e., 7.5 to 6.5 (Under the condition resolution is 1 V).

### (6) Temperature Sensitivity

As DAC circuit consists of temperature sensitive components like resistor, reference voltage source, OP-AMP, SPDT switches etc. As temperature changes (increases or decreases), characteristics of these components changes and hence obtained analog output voltage for any fixed digital input changes.

It is defined as—

“Change in output voltage from its expected value in respect of temperature and is specified in terms of  $\pm \text{ppm}/^\circ\text{C}$ .”

## 6.4 CLASSIFICATION OF DAC

Digital to analog converter can be of two types—

- (1) Weighted resistor type DAC
- (2) R-2R ladder type DAC (Binary ladder)

### (1) Weighted Resistor Type DAC—

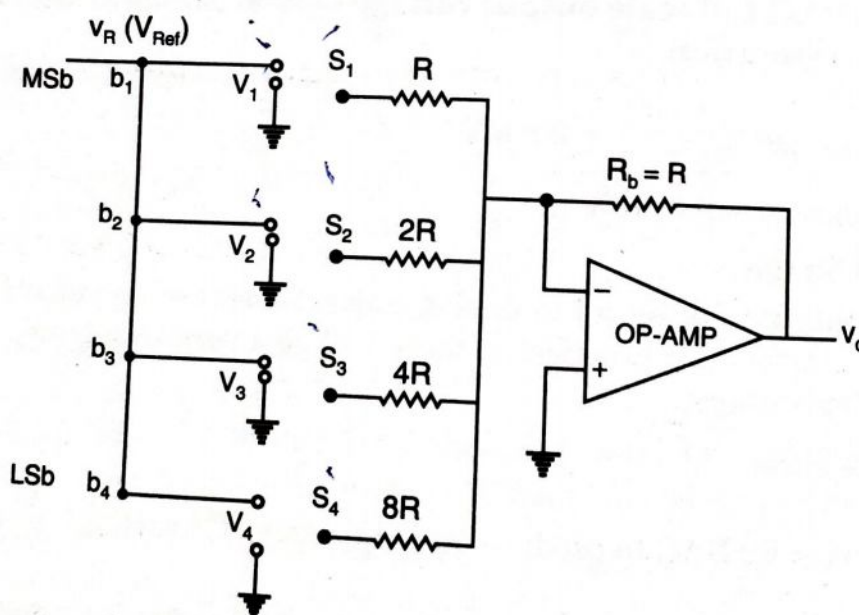


Fig. 6.7.

Weighted resistor type DAC consists of—

- (1) Reference voltage supply ( $V_R$ )
- (2) Resistor ladder network ( $R - 2R - 4R - 8R$ )
- (3) Digital input ( $b_1 b_2 b_3 b_4$ )
- (4) SPDT switches ( $S_1 S_2 S_3 S_4$ )
- (5) OPAMP (Acting as a summing amplifier)

### (1) Reference Voltage ( $V_R$ )

Reference voltage is taken as precise and stable so that an accurate analog output can be obtained.

D/A and A/D Converter  
(2) Resistor Ladder  
Starting with

Resistor value

It provides

e.g.— For

8 bit DAC

12 bit DAC

In General

(3) Digital Input

Digital input

Each binary

(4) SPDT Switch

SPDT switch

Case 1:

Then SPDT

resistor.

Case 2

Then SPDT

Hence,

e.g., If

Then

else

Then

e.g.,—

(5) Op-Amp

Op-Amp

Hence

Let's

Case

**(2) Resistor ladder Network ( $R - 2R - 4R - 8R$ )**

Starting with MSb resistor (which is connected to MSb bit)

⇓

Resistor values are increased by a factor of 2.

⇓

It provides desired weights in output voltage.

e.g.— **For 4 bit DAC** : Input resistors range from  $R$  to  $8R$

**8 bit DAC** : Input resistors range from  $R$  to  $128R$

**12 bit DAC** : Input resistors range from  $R$  to  $2048R$

**In General** : For  $N$  bit DAC : Input resistors range from  $R$  to  $2^{N-1}R$

**(3) Digital Input Data ( $b_1, b_2, b_3, b_4$ )**

Digital input data (binary) can range from 0 to  $N$  bits e.g.,  $b_1, b_2, b_3, \dots, b_N$ .  
Each binary bit can be assigned value higher 0 or 1.

**(4) SPDT (Single pole double throw switches) ( $s_1, s_2, s_3, s_4$ )**

SPDT switches  $s_1, s_2, s_3, s_4$  are controlled by  $b_1, b_2, b_3, b_4$  respectively.

Case 1: If data input is high

⇓

Then SPDT switches connects reference voltage ( $V_{Ref}$ ) to corresponding input resistor.

Case 2 : If data input is low

⇓

Then SPDT switch connects ground to corresponding I/P resistor.

Hence, we can define—

$$V_k = V_{Ref} b_k$$

e.g., If

$$b_k = 1$$

Then

$$V_k = V_{Ref}$$

else

$$b_k = 0$$

Then

$$V_k = 0$$

e.g.,—

$$V_1 = V_{Ref} b_1$$

$$V_2 = V_{Ref} b_2$$

$$V_3 = V_{Ref} b_3$$

$$V_4 = V_{Ref} b_4$$

**(5) Op-Amp (Summing Amplifier)**

OP-Amp is used as a summing amplifier

⇓

Hence, it produces weight sum of binary inputs.

Let's apply superposition theorem

Case 1  $b_1 = 1$

$$b_2 = 0$$

$$b_3 = 0$$

$$b_4 = 0$$

$$V_{01} = \frac{-R_f}{R} V_1$$

Case 2  $b_1 = 0$

$$b_2 = 1$$

$$b_3 = 0$$

$$b_4 = 0$$

$$V_{02} = \frac{-R_f}{2R} V_2$$

Case 3 :  $b_1 = 0$

$$b_2 = 0$$

$$b_3 = 1$$

$$b_4 = 0$$

$$V_{03} = \frac{-R_f}{4R} V_3$$

Case 4:  $b_1 = 0$

$$b_2 = 0$$

$$b_3 = 0$$

$$b_4 = 1$$

$$V_{04} = \frac{-R_f}{8R} V_4$$

Applying superposition theorem—

$$V_0 = V_{01} + V_{02} + V_{03} + V_{04}$$

$$V_0 = \frac{-R_f}{R} V_1 - \frac{R_f}{2R} V_2 - \frac{R_f}{4R} V_3 - \frac{R_f}{8R} V_4$$

$\Rightarrow$

$$V_0 = \frac{-R_f}{R} \left[ V_1 + \frac{V_2}{2} + \frac{V_3}{4} + \frac{V_4}{8} \right]$$

As

Hence

$$V_k = b_k V_{\text{Ref}}$$

$$V_0 = \frac{-R_f}{R} \left[ b_1 V_{\text{Ref}} + \frac{b_2 V_{\text{Ref}}}{2} + \frac{b_3 V_{\text{Ref}}}{4} + \frac{b_4 V_{\text{Ref}}}{8} \right]$$

$\Rightarrow$

$$V_0 = \frac{-R_f}{R} V_{\text{Ref}} \left[ b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8} \right]$$

$\Rightarrow$

$$V_0 = k V_{\text{Ref}} \left[ b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8} \right]$$

e.g., Let's take

and

Let's take  $b_1 b_2 b_3 b_4$  as 1011

In this way—

$$R_f = R$$

$$V_{\text{Ref}} = 8 \text{ V}$$

$\Rightarrow$

$\Rightarrow$

### Drawback

There is a large resistor in many bit (High MSb) resistor. It is very difficult. In other words, Hence, it is not suitable for large values.

### R - 2R Ladder

In this case, it is called as R-2R ladder.

MSb

Whole and  
Case 1: I

$$V_0 = -8 \left[ 1 + \frac{1}{4} + \frac{1}{8} \right]$$

$$V_0 = -8 \left[ \frac{8+2+1}{8} \right]$$

$$V_0 = -11 \text{ V}$$

### Drawback

There is a large difference in resistor values between LSb and MSb especially in many bit (High resolution) DAC. e.g., 10 bit DAC MSb resistor is  $R$  and LSb resistor is  $512 R$ .

It is very difficult to fabricate with a wide resistance range.

In other words fabrication cost will be also high.

Hence, it is preferable to take a circuit that uses resistance of fairly close values.

### R-2R Ladder DAC (Binary Ladder)

In this case, we use only two values of resistance either  $R$  or  $2R$ . Hence, it is called as R-2R ladder type DAC.

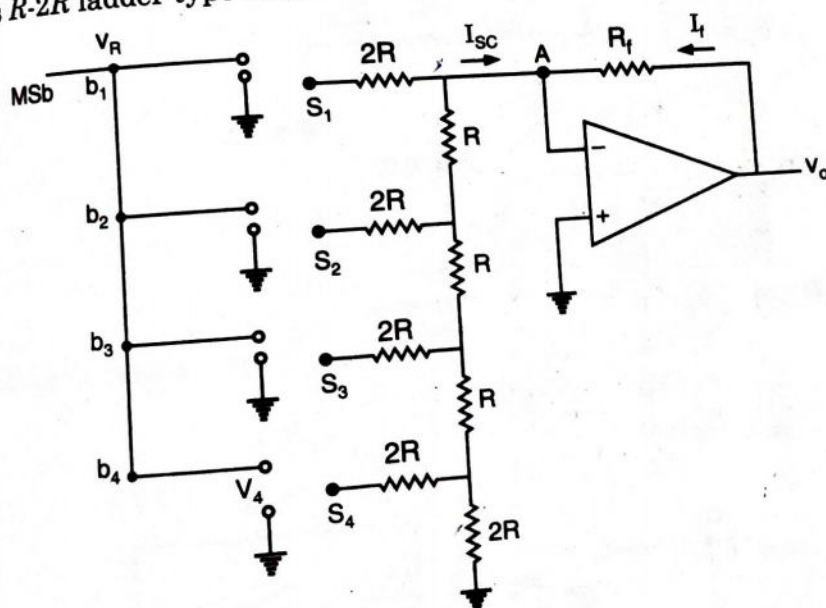


Fig. 6.8.

Whole analysis is divided in 4 cases

Case 1: Let  $b_1 = 1$

$$b_2 = 0$$

$$b_3 = 0$$

$$b_4 = 0$$

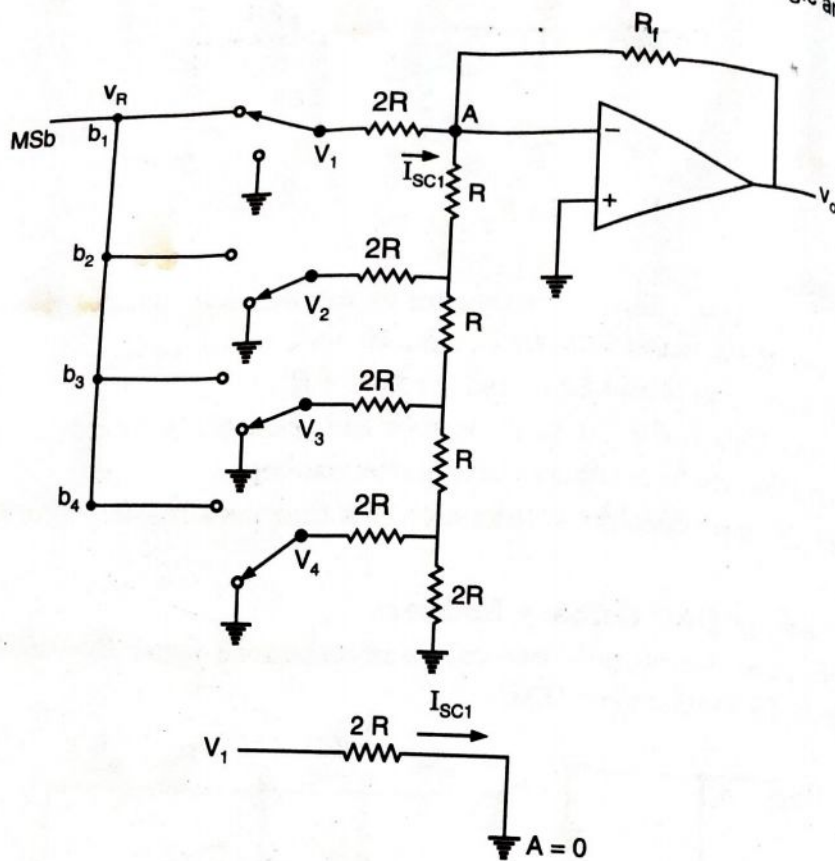
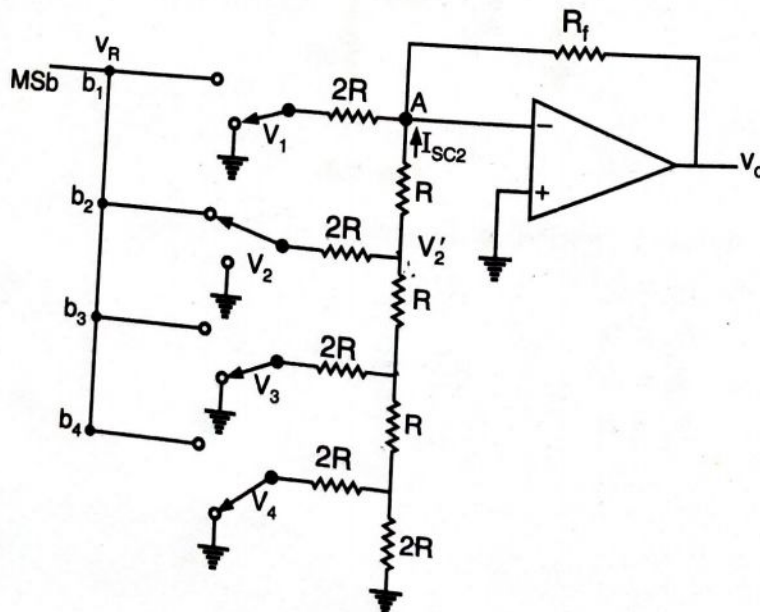


Fig. 6.9.

$$I_{SC1} = \frac{V_1}{2R}$$

Case 2: Let  $b_1 = 0$   
 $b_2 = 1$   
 $b_3 = 0$   
 $b_4 = 0$



Starting the ana

 $V_2$ 

By voltage d

Hence,

 $\Rightarrow$  $\Rightarrow$

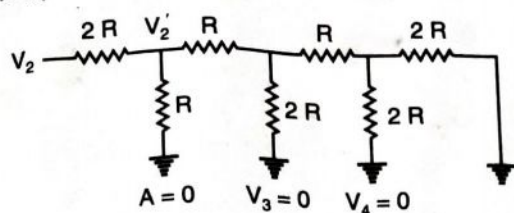


Fig. 6.10.

Starting the analysis with right hand side.

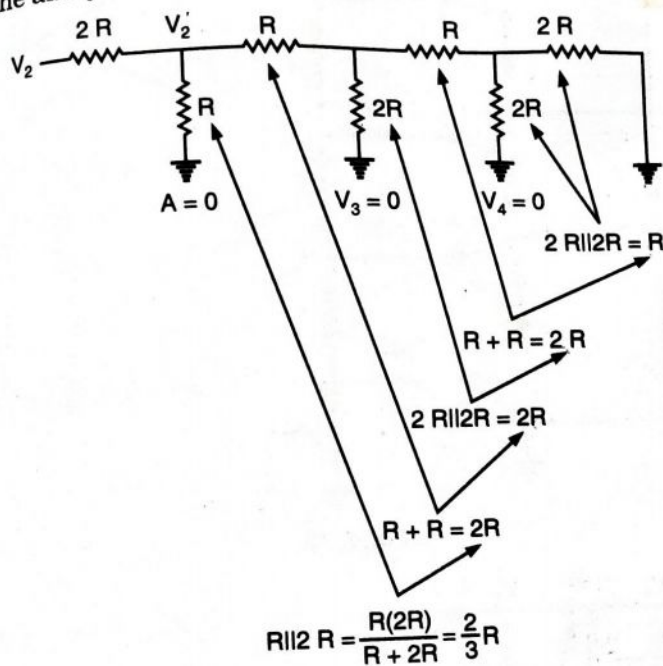


Fig. 6.11.

$$\frac{1}{R} = \frac{1}{2R} + \frac{1}{2R}$$

$$\frac{1}{R} = \frac{2}{2R}$$

By voltage dividing Rule

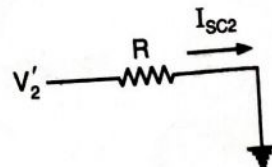
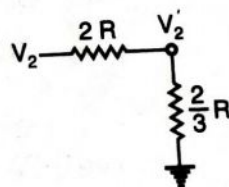
Hence, 
$$V_2' = \frac{\frac{2}{3}R}{2R + \frac{2}{3}R} V_2$$

$$\Rightarrow V_2' = \frac{2}{3}R \left( \frac{3}{8R} \right) V_2$$

$$V_2' = \frac{2V_2}{8} = \frac{1}{4}V_2$$

$$\Rightarrow I_{SC2} = \frac{V_2'}{R} = \left( \frac{V_2}{4} \right) \frac{1}{R} = \frac{V_2}{4R}$$

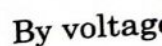
$$\boxed{I_{SC2} = \frac{V_2}{4R}}$$



D/A and A/D Conv  
By voltage c



⇒



By puttir



[Again starting the analysis  
with right side]



### Case 4:

By voltage dividing rule

$$V_x = \frac{\frac{10}{11}R}{2R + \frac{10}{11}R} V_3$$

$$\Rightarrow V_x = \left(\frac{10}{11}R\right) \left(\frac{11}{32R}\right) V_3$$

$$\Rightarrow V_x = \frac{10}{32} V_3 = \frac{5}{16} V_3$$

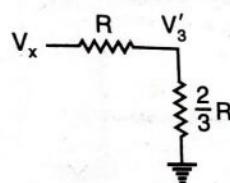


Fig. 6.14.

By voltage dividing rule

$$V'_3 = \frac{V_x \frac{2}{3}R}{R + \frac{2}{3}R} = V_x \left(\frac{2}{3}R\right) \times \left(\frac{3}{5R}\right) = V_x \left(\frac{2}{5}\right)$$

By putting value of  $V_x = \frac{5}{16} V_3$

$$\Rightarrow V'_3 = \frac{5}{16} V_3 \left(\frac{2}{5}\right) = \frac{V_3}{8}$$

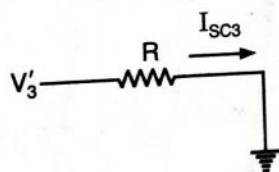


Fig. 6.15.

$$I_{SC3} = \frac{V'_3}{R} = \frac{V_3}{8R}$$

$$\Rightarrow \boxed{I_{SC3} = \frac{V_3}{8R}}$$

Case 4: Let

$$b_1 = 0$$

$$b_2 = 0$$

$$b_3 = 0$$

$$b_4 = 1$$

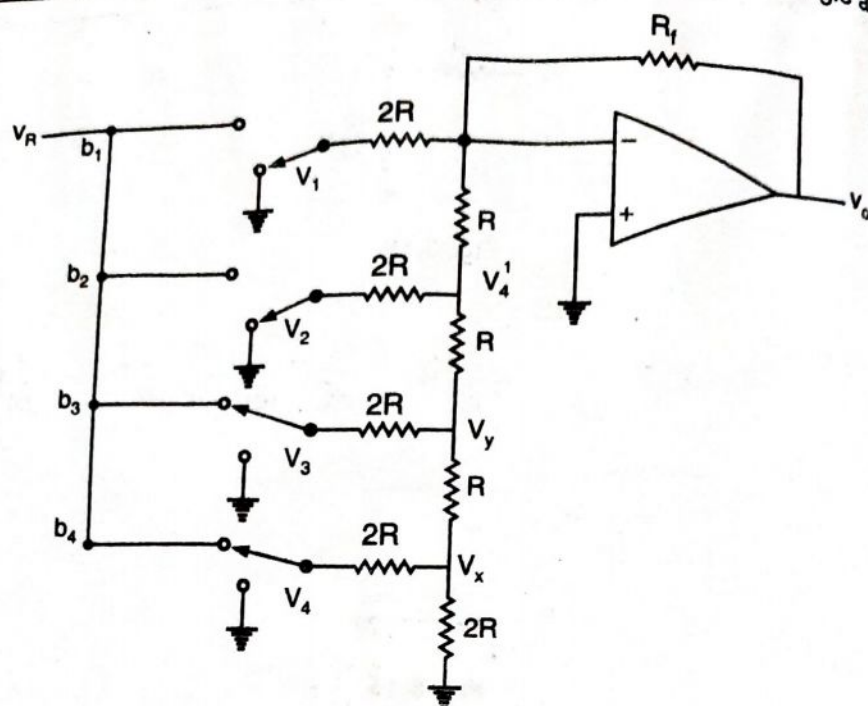


Fig. 6.16.

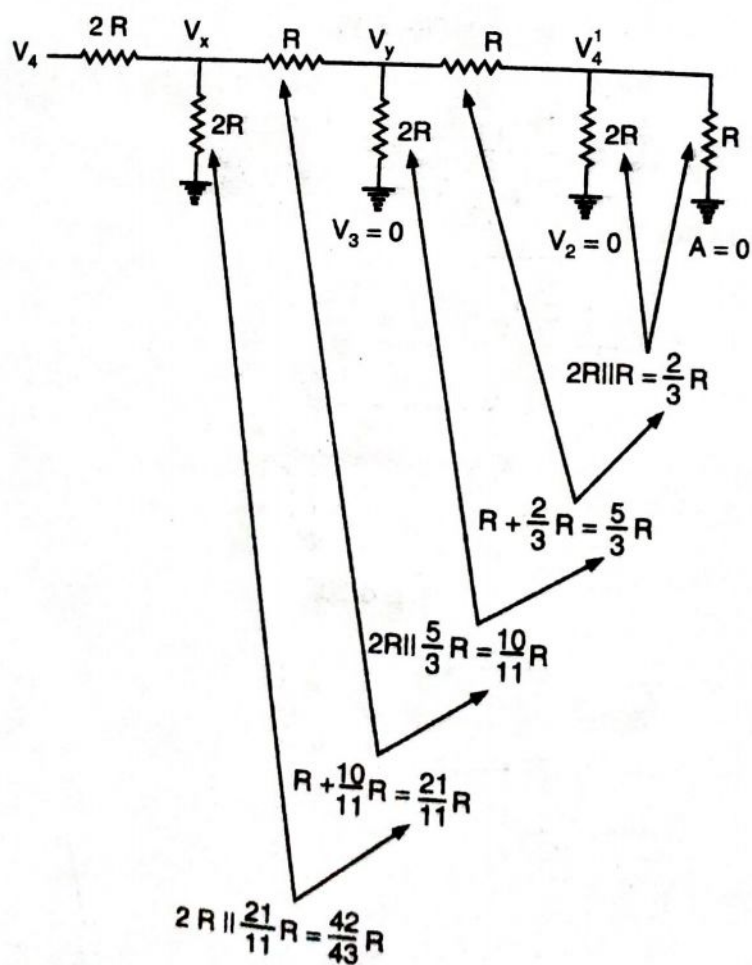


Fig. 6.17.

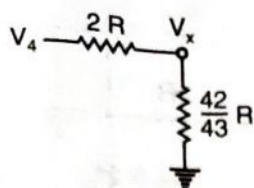


Fig. 6.18.

$$V_x = \frac{\frac{42}{43}R}{2R + \frac{42}{43}R} V_4 = \frac{42}{43}R \frac{43}{(86 + 42)R} V_4 = \frac{42}{128} V_4$$

$$\boxed{V_x = \frac{21}{64} V_4}$$

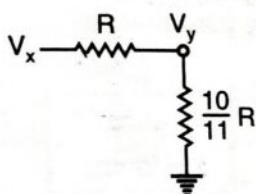


Fig. 6.19.

$$V_y = \frac{V_x \frac{10}{11}R}{R + \frac{10}{11}R} = V_x \left( \frac{10}{11} \right) \frac{11}{21}$$

$$\boxed{V_y = \frac{10}{21} V_x}$$

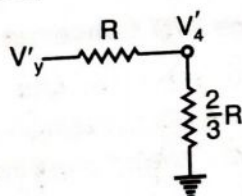


Fig. 6.20.

$$V_4' = \frac{V_y \frac{2}{3}R}{R + \frac{2}{3}R} = V_y \frac{2}{3} \frac{3}{5}$$

$$\boxed{V_4' = \frac{2}{5} V_y}$$

$$V_4' = \frac{2}{5} V_y = \frac{2}{5} \left( \frac{10}{21} V_x \right) = \frac{4}{21} V_x = \frac{4}{21} \left( \frac{21}{64} V_4 \right)$$

$$V_4' = \frac{1}{16} V_4$$