

### 4.32.1. Shift Register Counters

It is defined as "shift registers with the serial outputs connected back to the serial inputs in order to produce a particular sequence."  
These registers are classified as counters because they exhibit a specified sequence of states.  
They are of two types

- (1) Ring counter
- (2) Johnson counter

### 4.32.2. Ring Counter

Ring counter is an synchronous counter in which last output (i.e., LSB) is feeded back to the input of the first flip-flop as shown in below diagram. As it is synchronous one, the clock pulse of all flip-flop is same.]

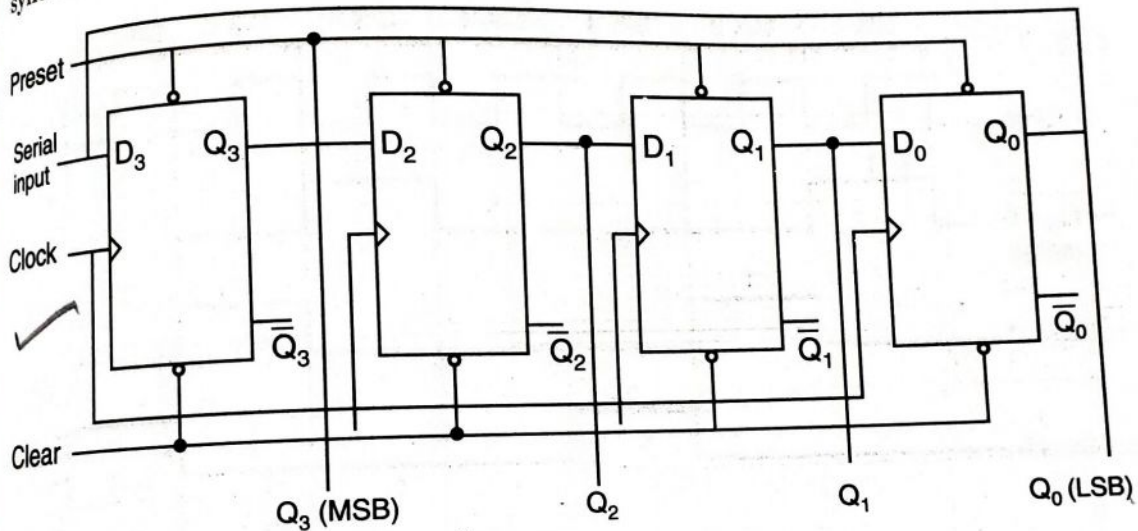
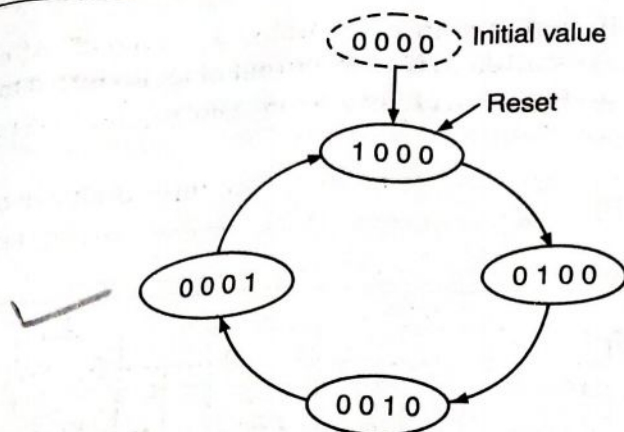


Fig. 4.154.

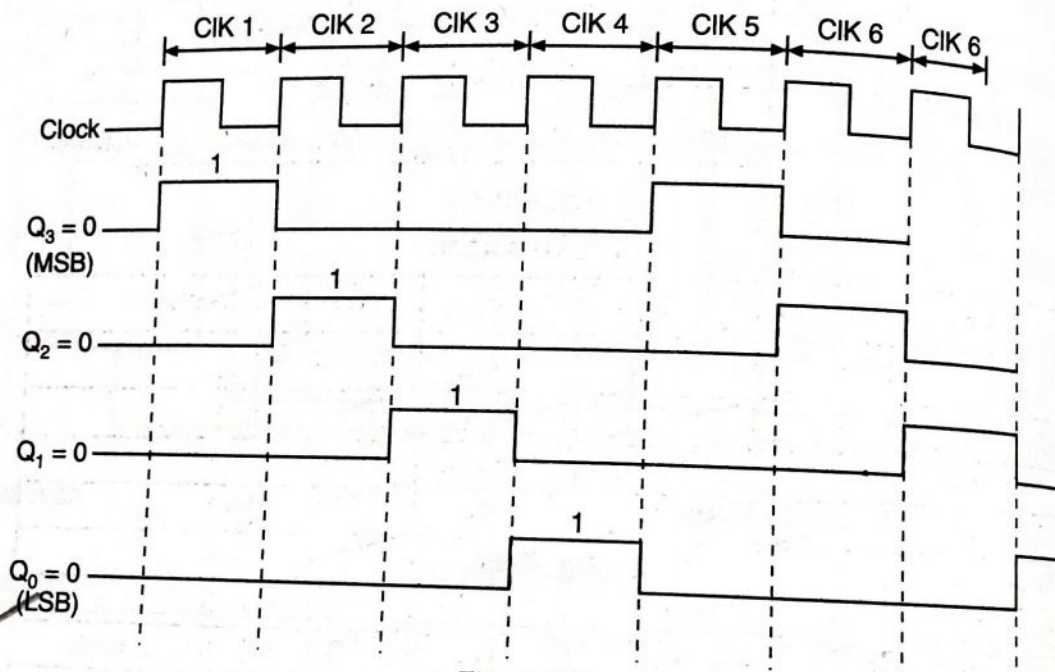
| ✓                    | $Q_3$<br>(MSB) | $Q_2$ | $Q_1$ | $Q_0$<br>(LSB) | Counts                |
|----------------------|----------------|-------|-------|----------------|-----------------------|
| On Reset (Initially) | 0              | 0     | 0     | 0              | 0                     |
| 1st clock pulse      | 1              | 0     | 0     | 0              | 1                     |
| 2nd clock pulse      | 0              | 1     | 0     | 0              | 2                     |
| 3rd clock pulse      | 0              | 0     | 1     | 0              | 3                     |
| 4th clock pulse      | 0              | 0     | 0     | 1              | 4                     |
| 5th clock pulse      | ①              | 0     | 0     | 0              | Recycle or repetition |

The output of FF-3 is set to one on arrival of 1st clock pulse with the help of preset input and on reset all flip-flop are cleared to '0' with clear input = '0'.  
As the positive edge of clock is arrived flip-flop 1 and so on. flip-flop 2 and similarly flip-flop 2 gives its output to the flip-flop 1 and so on.  
The working can be easily understand by the help of state diagram and waveforms as shown below.





**Fig. 4.155.** State diagram of 4 bit ring counter



**Fig. 4.156.**

**Note:** If we use 4 flip-flop then number of states i.e., modules is '4' (i.e., counts from 0, 1, 2, 3 and then repeats).

### Advantages of Ring Counter

The major advantage of a ring counter over a binary counter is a self decoding counter. No extra decoding circuit is needed to determine what state the counter is in.

### Disadvantage of Ring Counter

Ring counter is very inefficient in terms of state usage. Let us take an example—In MOD-4 counter, maximum states possible are 16 (as '4' flip flops are used so,  $2^4$  i.e., 16 output/states are present) out of which only '4' states are used. So it is really inefficient in terms of states usage.

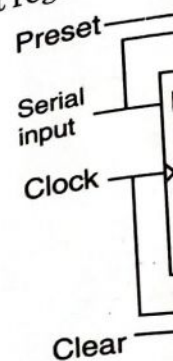
#### 4.33 JOHNSON COUNTER (TWISTED RING COUNTER/MOEBIUS COUNTER)

**COUNTER (TWISTED RING COUNTER/MOEBIUS COUNTER)**  
This counter is similar to Ring Counter but only one difference is there that in it we feedback  $\bar{Q}_0$  instead of  $Q_0$  to the serial input ( $D_3$ ).

Sequential Logic C  
Initially all

Initially all pulse, the output of the output clock

every eight clock  
A positive e  
inter (SI



|             |
|-------------|
| Clock       |
| Initially   |
| Clock - 1st |
| Clock - 2nd |
| Clock - 3rd |
| Clock - 4th |
| Clock - 5th |
| Clock - 6th |
| Clock - 7th |
| Clock - 8th |

The stat



Initially all the flip-flops are in reset state i.e., "0 0 0 0". After each clock pulse, the output of  $Q_3$  is shifted to  $Q_2$ , the output of  $Q_2$  is shifted to  $Q_1$ ,  $Q_1$  to  $Q_0$  and the output of  $\bar{Q}_0$  is shifted to  $Q_3$  and so on. This sequence is repeated after every eight clock pulses.

A positive edge triggered 4-bit twisted ring counter is shown below. It is an shift register (SIPO) in which last output ( $\bar{Q}_0$ ) is feedback to the serial input ( $D_3$ ).

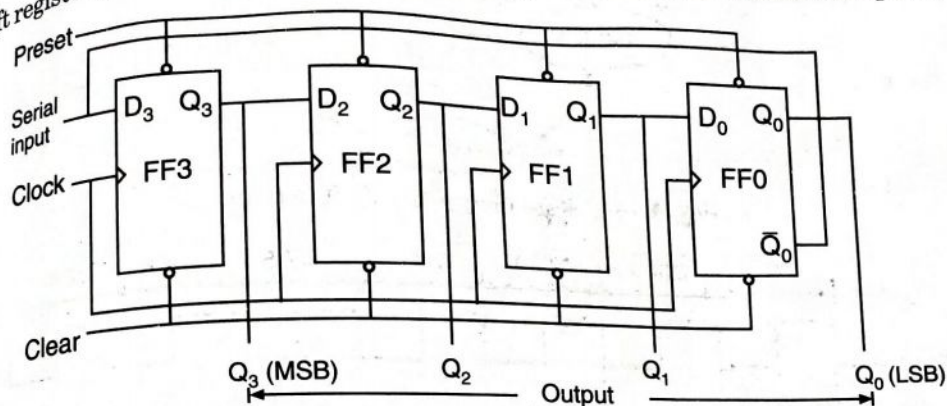


Fig. 4.157.

Truth Table

| Clock       | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | Counts                  |
|-------------|-------|-------|-------|-------|-------------------------|
| Initially   | 0     | 0     | 0     | 0     | 0                       |
| Clock - 1st | 1     | 0     | 0     | 0     | 1                       |
| Clock - 2nd | 1     | 1     | 0     | 0     | 2                       |
| Clock - 3rd | 1     | 1     | 1     | 0     | 3                       |
| Clock - 4th | 1     | 1     | 1     | 1     | 4                       |
| Clock - 5th | 0     | 1     | 1     | 1     | 5                       |
| Clock - 6th | 0     | 0     | 1     | 1     | 6                       |
| Clock - 7th | 0     | 0     | 0     | 1     | 7                       |
| Clock - 8th | 0     | 0     | 0     | 0     | 0 → Repeats or Recycles |

The state diagram is shown as follows:

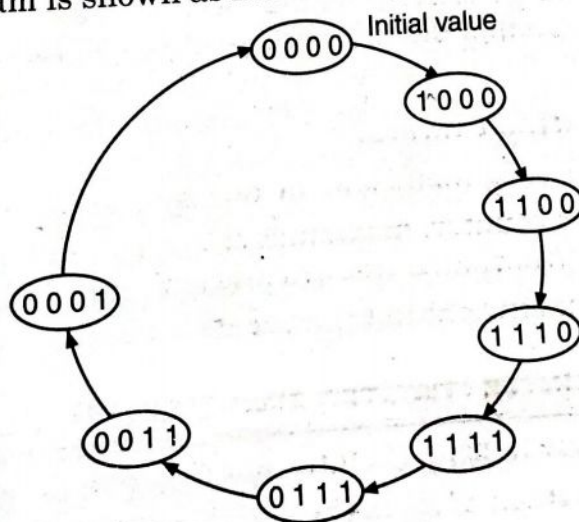


Fig. 4.158.



**Note:** As shown above, twisted ring counter is capable of counting 8 states (if 4 flip flops are used). Hence if 'N' flip-flop twisted ring counter is there, then it counts  $2N$  states which is double of ring counter (If N flip-flop are there, then it counts 'N' states)

The waveform is shown as below:

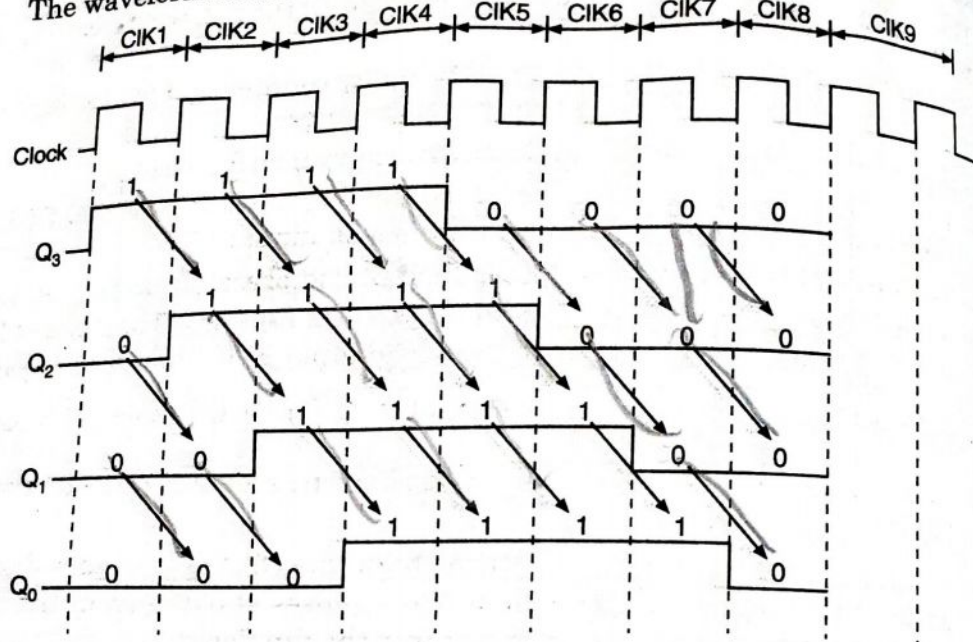


Fig. 4.159.

#### Disadvantage of Johnson counter

In Johnson counter maximum available states are not fully utilized. As in 4-bit twisted ring counter/Johnson counter only 8 of 16 states are being used.

#### 4.34 COMPARISON BETWEEN RING COUNTER AND JOHNSON COUNTER

- A ring counter is a circular shift register with only one flip-flop being set any particular time, all others are cleared. The single bit is shifted from one flip flop to the other to produce the sequence of timing signals whereas Johnson ring counter is modified ring counter where the complement output of the last flip flop is connected to the input of the first flip flop.
- Ring counter is also known as conventional ring counter whereas Johnson ring counter is also known as twisted ring counter.
- In ring counter it requires at least one flip flop present to logic '1' and at least one flip flop reset to logic 0 whereas Johnson counter may start with all its flip flop in the reset condition.
- In ring counter the number of states is 'N' where 'N' is the number of flip flops whereas in case of Johnson counter the number of states is  $2N$ .
- Ring counter is known as Divide by N counter whereas Johnson counter is known as Divide by  $2N$  counter.

#### 4.35 PRESETTABLE COUNTERS

Presettable counters are the type of counters that can count from any desired state.

Sequential Logic C  
In case of U  
starts from 111  
from either 000  
desired state.

This is done  
before the coun

We can sta  
001, 010, 011, 1

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inputs v

— The des  
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