gic and Design ripple counter from 0 - 5 i.e., Q, 0 0 0 1 0 1 0 0

0

1

0

1

1

nter counts

0

0 1

0 0

Sequential Logic Circuits and its Design Shift Register Counters

4.32.1. defined as "shift room." 32.1. Shift registers with the serial outputs connected back to the

It is delines in order to produce a particular sequence."

priging inputs in order to produce a particular sequence."

priging inputs registers are classifed as countered to the serial outputs. is inputs in registers are classifed as counters because they exhibit a specified these of states. sequence of states.

They are of two types

(1) Ring counter

(2) Johnson counter

4.32.2. Ring Counter 4.32.2.

Ring counter is an synchronous counter in which last output (i.e., LSB) is feeded

Ring to the input of the first flip-flop as shown in the counter in the counter is an expectation. Ring counted input of the first flip-flop as shown in below diagram. As it is back to the clock pulse of all flip-flop is same.

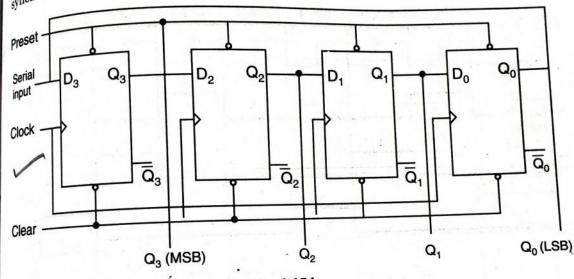


Fig. 4.154.

	Q <sub>3</sub> (MSB)	$\mathbf{Q_2}$	$Q_1$	Q <sub>0</sub> (LSB)	Counts
On Reset (Initially)	0-	0_	0_	0	0
	_ <u>`</u> `	<b>1</b> 0	0	0	1
1st clock pulse	1		<b>10</b>	0	2
2nd clock pulse	0		1	0	3
3rd clock pulse	0	0	1	1	4
4th clock pulse	0	0	-0 <u>)</u>	0	Recycle
5th clock pulse	(1)	<b>0</b>	-0		or repetition

The output of FF-3 is set to one or arrival of 1st clock pulse with the help of preset input and on reset all flip-flop are cleared to '0' with clear input= '0'.

As the positive edge of clock is arrived flip-flop with shifts its output to the Positive edge of clock is allived in the flip-flop 1 and so on.

The working can be easily understand by the help of state diagram and waveforms as shown below.

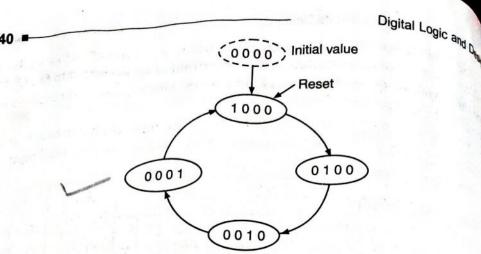
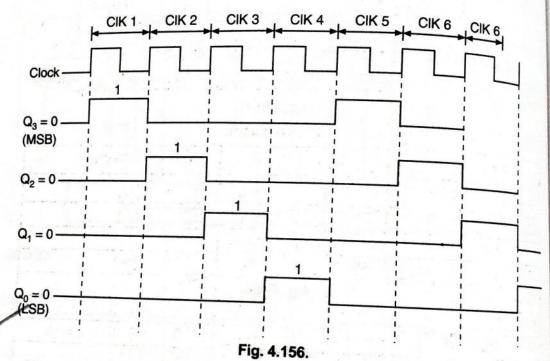


Fig. 4.155. State diagram of 4 bit ring counter



Note: If we use 4 flip-flop then number of states i.e., modules is '4' (i.e., counts from 0, 1, 2, 3 and then repeats).

## **Advantages of Ring Counter**

The major advantage of a ring counter over a binary counter is a self decoding counter. No extra decoding circuit is needed to determine what state the counter is in.

# Disadvantage of Ring Counter

Ring counter is very inefficient in terms of state usage. Let us take an male\_In MOD 4 example—In MOD-4 counter, maximum states possible are 16 (as '4' flip flops are used so. 24 i.e. 16 output) are used so, 24 i.e., 16 output/states are present) out of which only '4' states are used. So it is really inefficient in the states are present out of which only '4' states are used. So it is really inefficient in terms of states usage.

# 4.33 JOHNSON COUNTER (TWISTED RING COUNTER/MOEBIUS COUNTER)

This counter is similar to Ring Counter but only one difference is there that in the feedback  $\bar{Q}_{a}$  instead of  $Q_{a}$  in it we feedback  $\bar{Q}_0$  instead of  $Q_0$  to the serial input  $(D_3)$ .

Sequential Logic C Initially all pulse, the outpu and the output o every eight clock A positive e shift register (SI Presetserial input Clock

> Clock Initially Clock - 1st Clock - 2nd Clock - 3rd

Clear

Clock - 6th Clock - 7th

Clock - 4th

Clock - 5th

Clock - 8th

The stat

CIK 6

Saquential Logic Circuits and its Design all the flip-flops are in reset state i.e., "0 0 0 0". After each clock initially output of  $Q_3$  is shifted to  $Q_2$ , the output of  $Q_3$  is shifted to  $Q_4$ . pulse, the output of  $\overline{Q_0}$  is shifted to  $\overline{Q_0}$ , the output of  $\overline{Q_0}$  is shifted to  $\overline{Q_0}$ , and so on. This sequence: the output of  $\bar{Q}_0$  is shifted to  $Q_3$  and so on. This sequence is repeated after and the output of  $\bar{Q}_0$  is shifted to  $\bar{Q}_1$ ,  $\bar{Q}_1$  to  $\bar{Q}_0$  and so on. This sequence is repeated after and the output of  $\bar{Q}_0$  is shifted to  $\bar{Q}_1$ ,  $\bar{Q}_1$  to  $\bar{Q}_0$  and so on. This sequence is repeated after and  $\bar{Q}_1$  of  $\bar{Q}_1$  is shifted to  $\bar{Q}_2$  is shifted to  $\bar{Q}_1$ ,  $\bar{Q}_1$  to  $\bar{Q}_0$  and so on. This sequence is repeated after and  $\bar{Q}_1$  is shifted to  $\bar{Q}_2$  is shifted to  $\bar{Q}_1$ . every eight clock pulses.

Probabilitive edge triggered 4-bit twisted ring counter is shown below. It is an A positive (SIPO) in which last output  $(\overline{O}_{i})$  is facilly a A  $P^{0SlUV}$  (SIPO) in which last output ( $\overline{Q}_0$ ) is feedback to the serial input ( $D_3$ ).

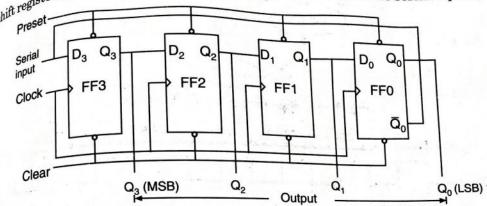


Fig. 4.157.

#### **Truth Table**

Clock	$Q_3$	$\mathbf{Q_2}$	$Q_1$	$Q_{\bar{0}}$	Counts
Initially	0_	0_	0_	0	0
Clock - 1st	1_	<b>~</b> 0 <b>~</b>	<b>^</b> 0	0	1
Clock - 2nd	1_	1	0	0	2
Clock - 3rd	1_	1_	1_	0	. 3
Clock - 4th	1	1_	1_	1	4
Clock - 5th	0,	1_	1	1	5
Clock - 6th	0_	0_	1_	1	6
	0.	Ó_	0_	1	7
Clock - 7th Clock - 8th	0	0	0	0	$0 \rightarrow \text{Repeats or}$ Recycles

The state diagram is shown as follows:

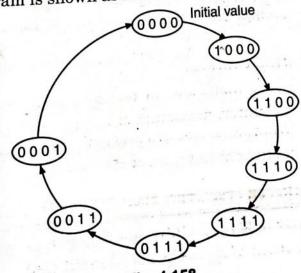


Fig. 4.158.

es is '4' (i.e.,

elf decoding the counter

us take an 4' flip flops 'states are

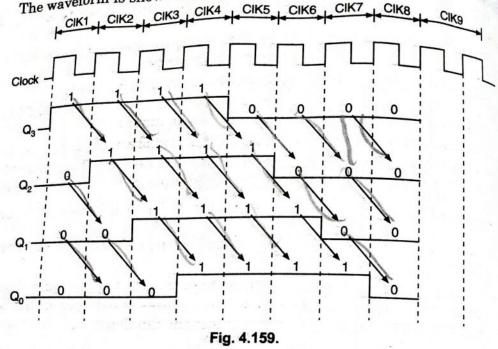
JNTER)

ere that in

Digital Logic and De Note: As shown above, twisted ring counter is capable of counting 8 stage Note: As shown above, twisted ring counter is there are used). Hence if 'N' flip-flop twisted ring counter (If N flip-flop as there are used).

Note: As shown above, twisted ring counter is there is there if 'N' flip-flop twisted ring counter is there is there if 4 flip flops are used). Hence if 'N' flip-flop counter (If N flip-flop are there, the states which is double of ring counter (If N flip-flop are there, the states which is double of ring counter (If N flip-flop are there). (if 4 flip flops are used). Hence it (if N flip flop are there, the it counts 2N states which is double of ring counter (If N flip flop are there, the it counts 2N states) it counts 'N' states)

The waveform is shown as below:



### Disadvantage of Jonson counter

In Johnson counter maximum available states are not fully utilized. As in 4-bit twisted ring counter/Johnson counter only 8 of 16 states are being used.

# 4.34 COMPARISON BETWEEN RING COUNTER AND JOHNSON COUNTER

- A ring counter is a circular shift register with only one flip-flop being set any particular time, all others are cleared. The single bit is shifted from one flip flop to the other to produce the sequence of timing signals whereas Johnson ring counter is modified ring counter where the complement output of the last flip flop is connected to the input of the first flip flop.
- Ring counter is also known as conventional ring counter wheras Johnson ring counter is also known as twisted ring counter.
- In ring counter it requires at least one flip flop present to logic '1' and at least one flip flop reset to logic O whereas Johnson counter may start with all its flip flop in the reset condition.
- In ring counter the number of states is 'N' where 'N' is the number of flip flops whereas in case of Johnson counter the number of states is 2N.
- Ring counter is known as Divide by N counter whereas Johnson counter is known as Divide by 2N counter.

#### PRESETTABLE COUNTERS 4.35

Presettable counters are the type of counters that can count from any desired state. state.

Sequential Logic C In case of U starts from 111 from either 000 desired state. This is done

before the coun We can sta 001, 010, 011, A presetta

\_ Here th inputs v The des where v

input is activat throug

inputs When and co enter

The cir

Clo Inp