$$\Delta t = \frac{n}{f}$$

where f = clock frequency in MHz
n = number of stages
Δt = time delay in μs

e.g. 4-bit register having clock frequency of 2 MHz, calculate the time delay
The time delay is given as

$$\Delta t = {}^{n}\!/_{f} = \frac{4}{2}$$

$$\Delta t = 2\mu s$$

4.31 COUNTER

Counter is special sequential device which is used to count the clock pulses.

A counter have number of binary state which progress in defined fixed sequential manner.

Or

A counter is an sequential machine that is constructed with the help of flip-flop and it changes its state according to the state diagram.

Or

A counter is basically a register that is capable of counting the number of clock pulses that are available at its clock input.

The counting of counter may be ascending, descending or in any manner defined by the designer.

For example:

A single J-K flip-flop can acts as an counter which counts two states as shown in below diagram.

When positive edge of clock is arrived then the J-K flip-flop changes its state from 0 to 1 or 1 to 0.

Let us assume initially the flip-flop is in reset condition *i.e.*, $Q_{n+1} = 0$ and we apply the input $J = K = 1$ hence the output is given as

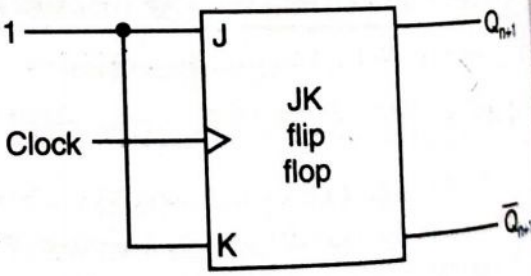


Fig. 4.128.

$$Q_{n+1} = \bar{Q}_n$$

where Q_{n+1} = Next state
Q_n = Present state

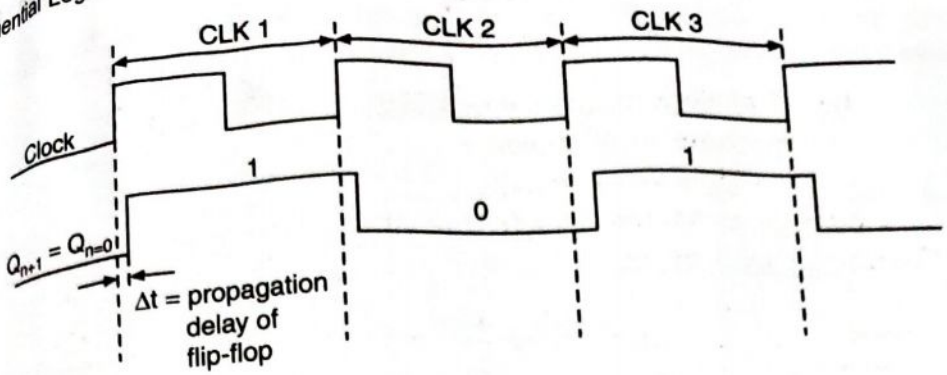


Fig. 4.129. Waveform of 1 bit counter

State Diagram: For single bit counter

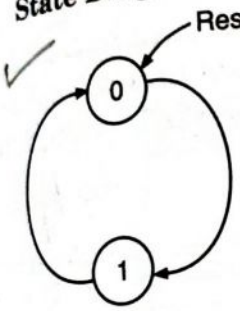


FIG. 4.130.

Truth Table

Clock	*Output* (Q_{n+1})	
↑	1	
↑	0	
↑	1	repeating sequence

State diagram consist of circle which contains the binary value.

Arrows in state diagram show the progress sequence of the counter. State is changed on arrival of clock pulse. For each clock pulse one state is changed.

Counter can be classified on the basis of following factors.

(*i*) Number of output bits or Number of flip-flop.

(*ii*) Number of states or modulus counter.

(*iii*) Single mode and multimode counter.

(*iv*) Synchronous and Asynchronous counter.

4.31.1. Number of Output Bits or Number of Flip-Flop

Counters can be classified on the basis of flip-flop used. One flip-flop output is equivalent to one bit of the counter. So, it is also known as binary counters. According to this criteria the flip-flop are

(*i*) **Single bit Binary Counter:** Single bit counter consist of two state 0, 1 as shown below in state diagram.

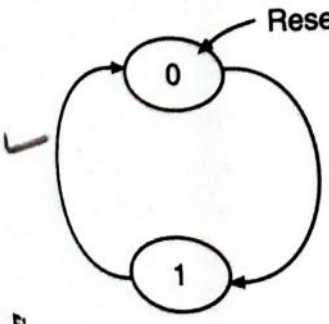


Fig. 4.131. State diagram of 1 bit counter

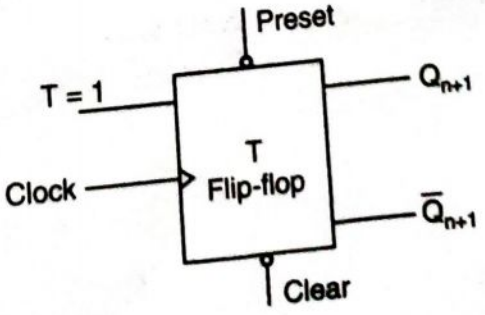


Fig. 4.132.

For single bit counter the input of T is high and the state is changed when positive edge of clock is arrived. Initially output is considered as '0'.

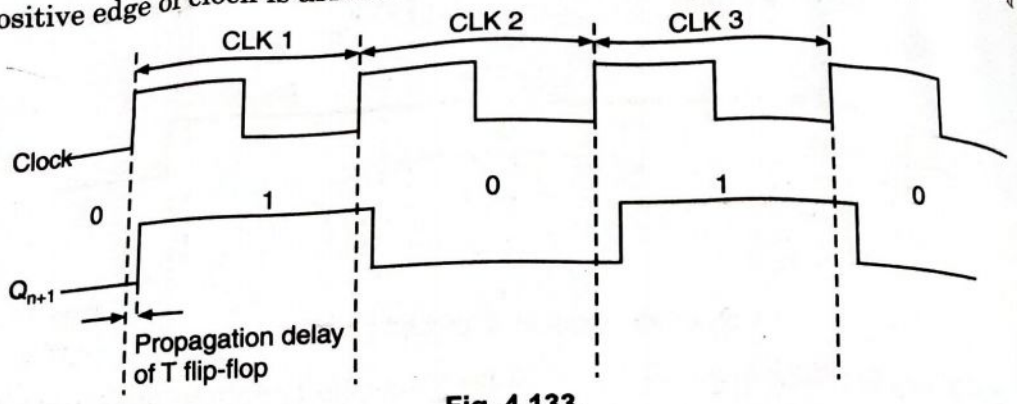


Fig. 4.133.

Truth Table

Clock	*Output* (Q_{n+1})
↑	1
↑	0
↑	1 repeating sequence

(*ii*) **2-bit Counter:** As the name suggested two bit counter consist of two flip-flop arranged in given below manner.

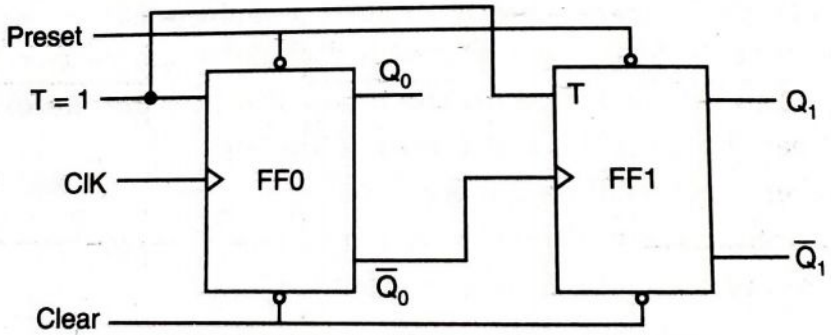


Fig. 4.134. 2-bit Ripple/Asynchronous Counter

2-bit counter shown (Ripple) in above figure is an **asynchronous counter** in which all flip-flop are not Synchronized (means clock is not common to all flip flops).

Preset and clear inputs are used to set the output of counter *i.e.*, initialization to "0 0" or to "11" output. The input T of the flip-flop is always connected to high logic (means '1').

State Diagram

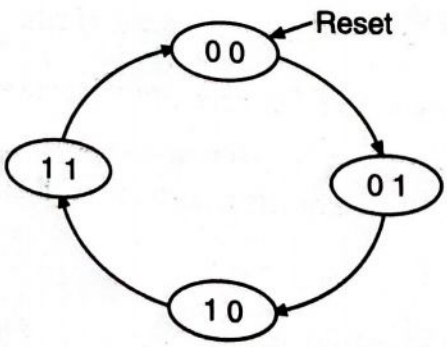


Fig. 4.135.

The four possible state of the 2 bit counter is shown in figure.

Truth Table

Clock pulse	Output	
	Q_1 (MSB)	Q_0 (LSB)
1.	0	0
2.	0	1
3.	1	0
4.	1	1
5.	0	0

→ repeatition/ recycle

From the above truth table it is cleared that 2 bit counter can counts four value and the functionality can be better understandable using waveform.

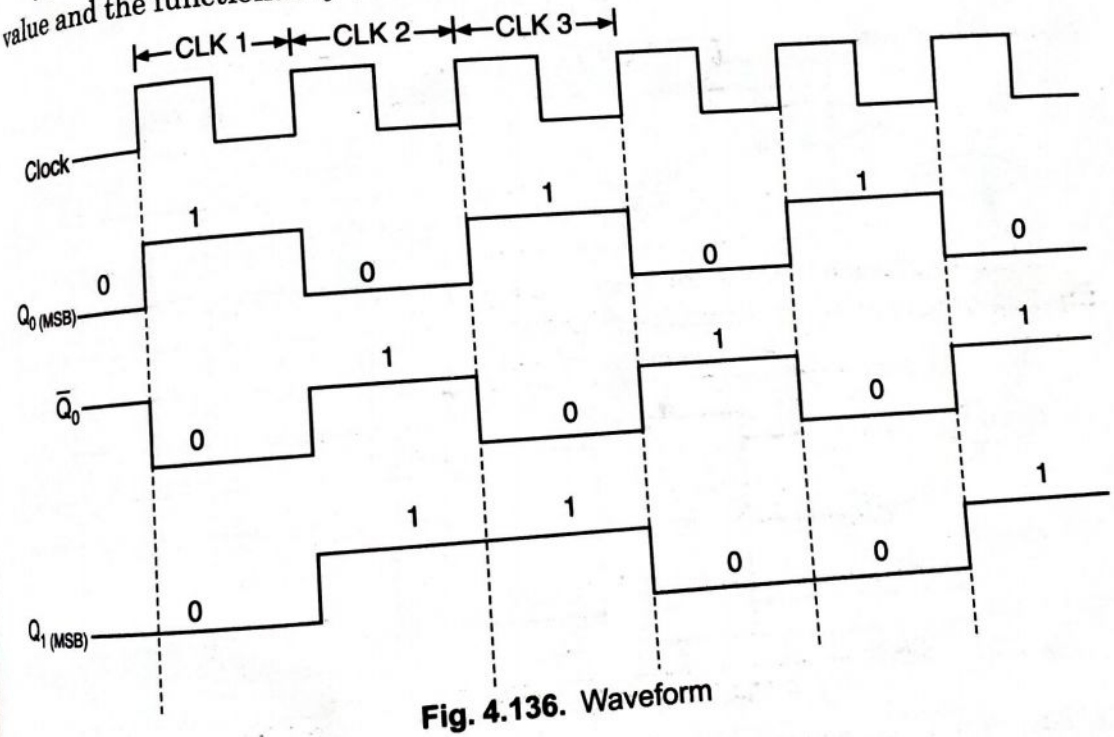


Fig. 4.136. Waveform

Working

The working of 2 bit Asynchronous counter can be easily understandable if we have knowledge about the working of T-flip-flop.

When input $T = 1$ then output $Q_{n+1} = \bar{Q}_n$ *i.e.*, Toggle hence on arrival of positive edge of clock pulse the output is just opposite of previous output.

The output $\bar{Q}_0$ is feeded to the clock input of flip-flop 1 hence when positive edge of $\bar{Q}_0$ is arrived then FF1 changes its state which can be better understandable from waveform figure.

(*iii*) **3-bit Counter:** 3 bit counter consist of 3 flip-flop as shown in below figure.

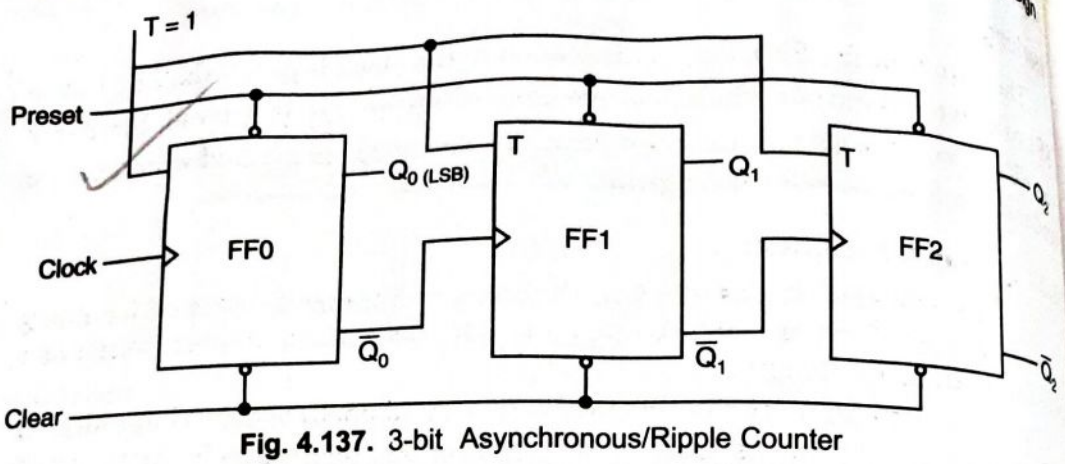
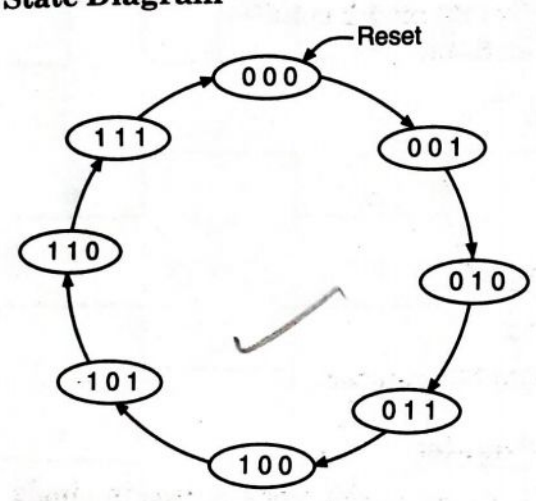


Fig. 4.137. 3-bit Asynchronous/Ripple Counter

Clock pulse is applied to FFO and the output, $\overline{Q}_0$ of the FFO is feeded to clock of FF-1 and similarly the output, $\overline{Q}_0$ of the FF-1 is feeded to clock of FF-2.

State Diagram



Truth Table

Q_2 (MSB)	Q_1	Q_0 (LSB)
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

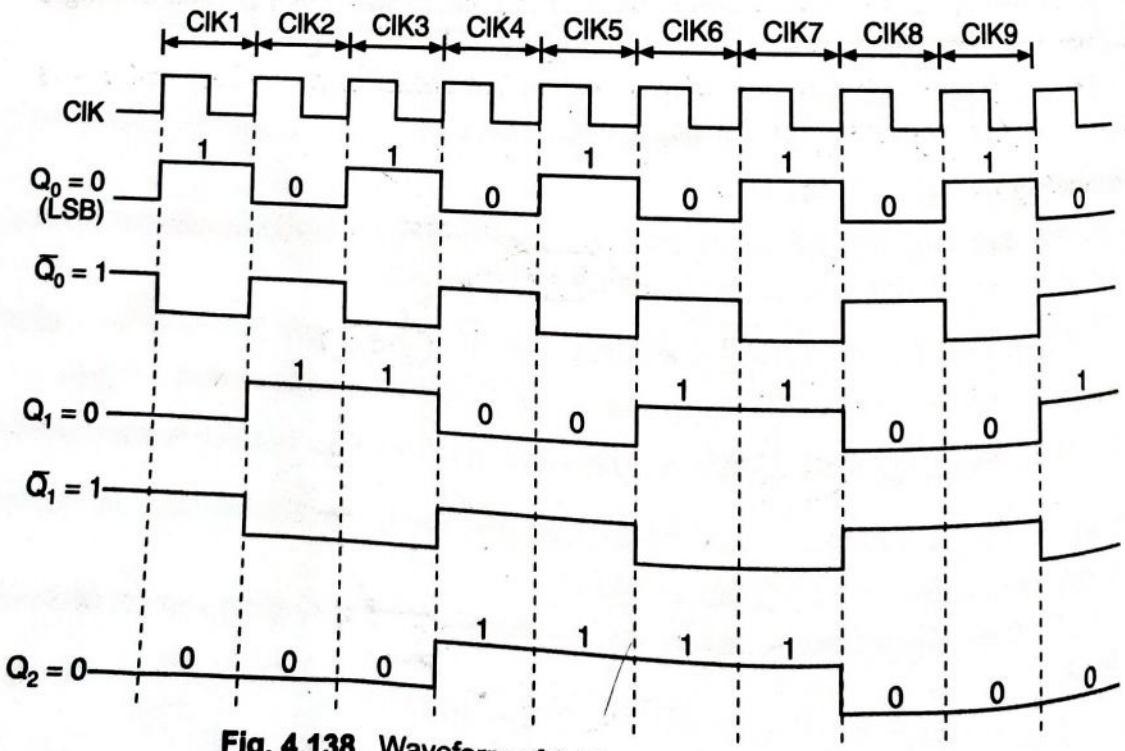


Fig. 4.138. Waveform of 3 bit asynchronous counter

Sequential Logic Circuit

Working

The output of th
FF1 calculate its ou
the FF2 calculates
understand from w

4.31.2. Modulu

Counter can a
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4.31.3. Sing

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Designing c

(*i*) State Dia

Working

The output of the FF0, *i.e.*, $\bar{Q}_0$ is feeded to the clock input of the FF1 hence FF1 calculate its output when positive edge of output $\bar{Q}_0$ is arrived. Similarly the FF2 calculates its output when positive edge of $\bar{Q}_1$ is arrived which can be understand from waveform diagram.

4.31.2. Modulus Counter

Counter can also be classified on the basis of number of states. Modulus-2 counter consist of two possible state, similarly modulus-4 counter consist of 4 possible states in an counter.

Modulus counter may be synchronouses or asynchronous. Generally for design modulus counter designer uses synchronous technique because design of an Synchronous counter is easier than asynchronous counter. e.g., MOD-5 denotes '5' states i.e., from 0 to 4 (000, 001, 010, 011, 100).

(*i*) **Modulus-2 Counter:** Modulus-2 counter consist of only two state (*i.e.*, 0 & 1) and only single flip-flop is enough to design mod-2 counter.

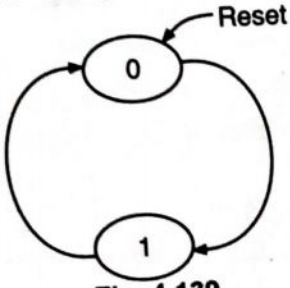


Fig. 4.139.

Hence mod-2 counter is similar to single bit counter.

4.31.3. Single Mode and Multimode Counter

A counter is said to be single mode if it counts the clock pulses in single manner *i.e.*, ascending order or in descending order.

For example: UP counter which counts its value in ascending order and recycle agains from its initial value.

Designing of up Counter:

(i) State Diagram

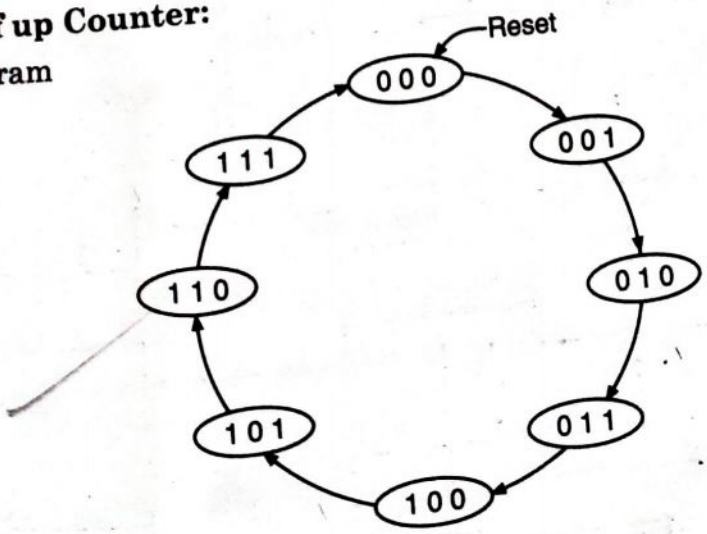


Fig. 4.140.

By using state diagram we construct the state variable assignment table as shown below.

In up counter the counter counts in ascending order of decimal number i.e., 0, 1, 2, 3, 4...

← Filled using Excitation table

Present State			Next State			D_2 (MSB)	D_1	D_0 (LSB)
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0			
0	0	0 0	0	0	1 1	0	0	1
0	0	1 1	0	1	0 2	0	1	0
0	1	0 2	0	1	1 3	0	1	1
0	1	1 3	1	0	0 4	1	0	0
1	0	0 4	1	0	1 5	1	0	1
1	0	1 5	1	1	0 6	1	1	0
1	1	0 6	1	1	1 7	1	1	1
1	1	1 7	0	0	0 0	0	0	0

The flip-flop is selected for construction of 3 bit up counter is D flip-flop.

Now use solve the equation of D_2, D_1, D_0 with the help of k-map and implement using DFF.

$D_2 (Q_2, Q_1, Q_0) = \Sigma m\ (3, 4, 5, 6)$

[for D_2 the value is high at minterms 3, 4, 5 & 6]

$D_1 (Q_2, Q_1, Q_0) = \Sigma m\ (1, 2, 5, 6)$

[for D_1, the vlaue is high at minterms 1, 2, 5 & 6]

$D_0 (Q_2, Q_1, Q_0) = \Sigma m\ (0, 2, 4, 6)$

[for D_0, the vlaue is high at minterms 0, 2, 4, 6]

For D_2

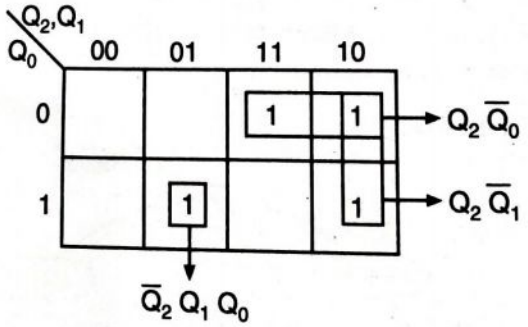


Fig. 4.141.

$$D_2 = \bar{Q}_2 Q_1 Q_0 + Q_2 \bar{Q}_0 + Q_2 \bar{Q}_1$$

$$= \bar{Q}_2 Q_1 Q_0 + Q_2 (\bar{Q}_0 + \bar{Q}_1)$$

For D_1

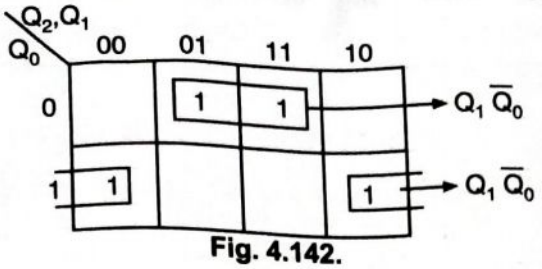


Fig. 4.142.

$$D_1 = Q_1 \bar{Q}_0 + \bar{Q}_1 Q_0$$
$$= Q_1 \oplus Q_0$$

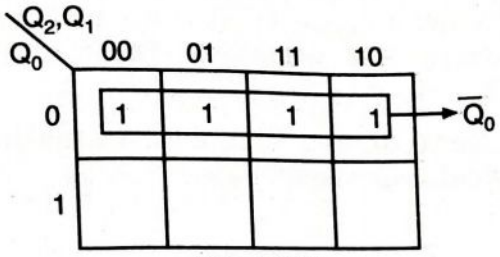


Fig. 4.143.

$$D_0 = \bar{Q}_0$$

Implement the equation of D_2, D_1, D_0 with help of Flip-Flop and combinational circuits as.

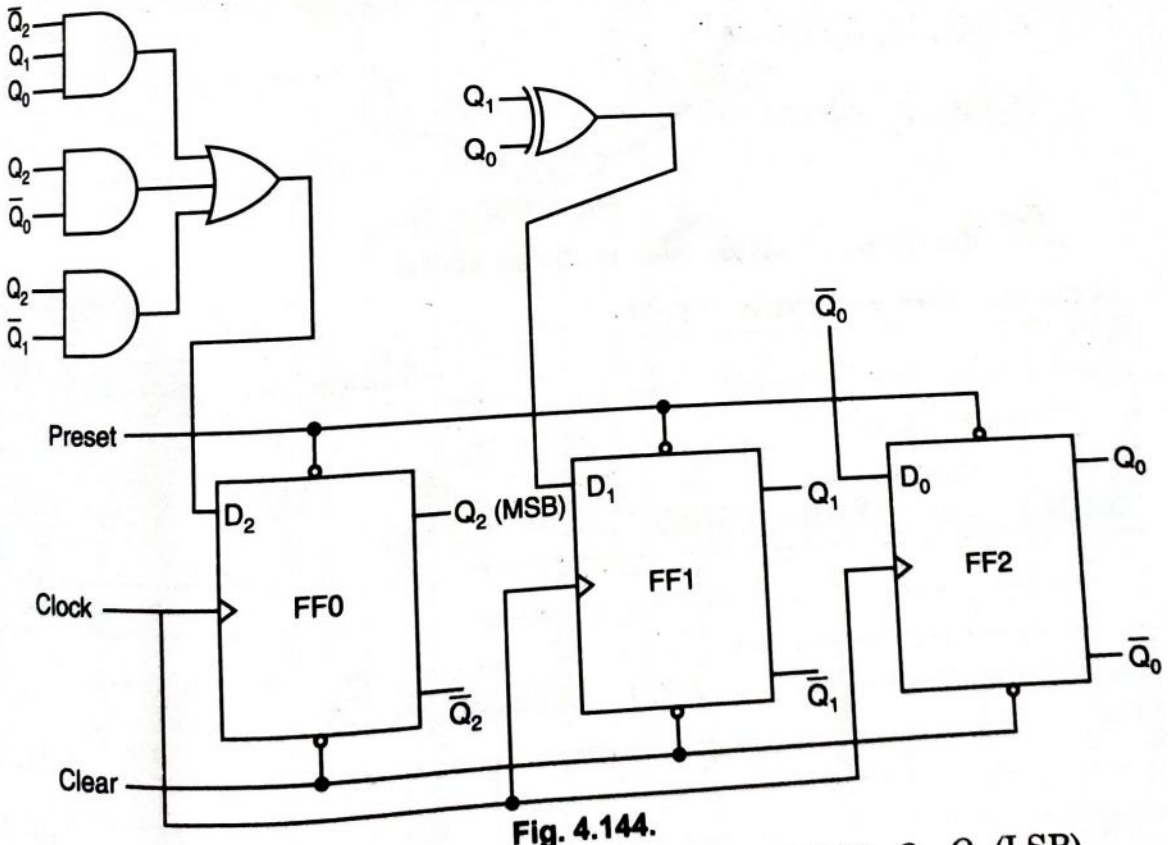


Fig. 4.144.

Output of the 3 bit up-counter is taken from Q_2 (MSB), Q_1, Q_0 (LSB).

Note: Excitation table for flip-flop is given as:

It is used for designing and determine the inputs from outputs (Q_n, Q_{n+1}).

Q_n (Present State)	Q_{n+1} (Next State)	S	R	J	K	T	D
		Flip-Flop		Flip-Flop		Flip-Flop	
0	0	0	×	0	×	0	0
0	1	1	0	1	×	1	1
1	0	0	1	×	1	1	0
1	1	×	0	×	0	0	1

Down Counter: Down counter is also an single mode counter which can counter its value in descending order only. Down counter works descending order of decimal number *i.e.*, 7, 6, 5, 4, 3, 2, 1, 0, 7, 6...

For designing the down counter first of all we make its state diagram and then state assignment table as shown below.

State Diagram:

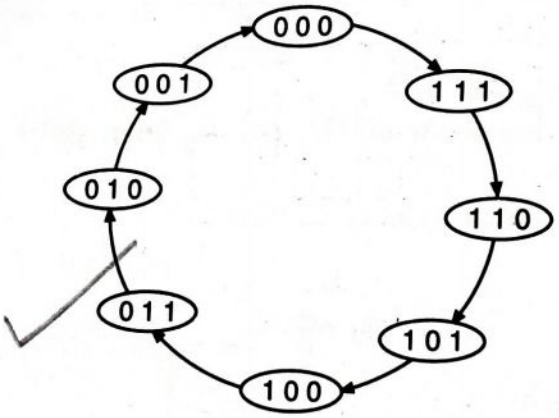


Fig. 4.145.

State diagram of 3 bit counter is shown above.

State variable assignment table

←Using Excitation Table→								
Present State			Next State					
Q_2 MSB	Q_1	Q_0 LSB	Q_2 MSB	Q_1	Q_0 LSB	D_2	D_1	D_0
0	0	0	1	1	1	1	1	1
1	1	1	1	1	0	1	1	0
1	1	0	1	0	1	1	0	1
1	0	1	1	0	0	1	0	0
1	0	0	0	1	1	0	1	1
0	1	1	0	1	0	0	1	0
0	1	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0

Now solve the equation for D_2, D_1, D_0 using k-map

$$D_2 (Q_2, Q_1, Q_0) = \Sigma m\ (0, 5, 6, 7)$$
$$D_1 (Q_2, Q_1, Q_0) = \Sigma m\ (0, 3, 4, 7)$$
$$D_0 (Q_2, Q_1, Q_0) = \Sigma m\ (0, 2, 4, 6)$$

For D_2

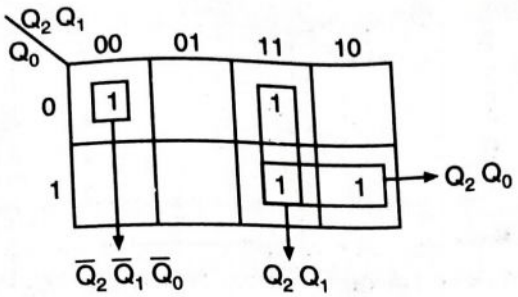


Fig. 4.146.

$$D_2 = \bar{Q}_2\, \bar{Q}_1\, \bar{Q}_0 + Q_2\, Q_1 + Q_2\, Q_0$$

For D_1

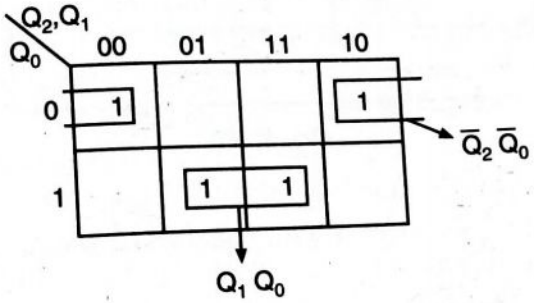


Fig. 4.147.

$$D_1 = Q_1\, Q_0 + \bar{Q}_1\, \bar{Q}_0$$
$$= Q_1 \odot Q_0$$

For D_0

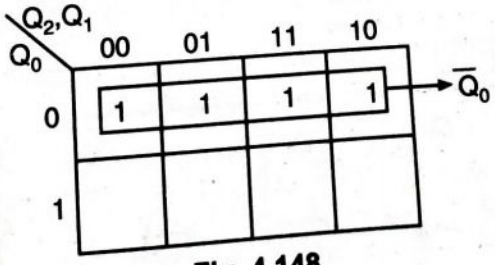


Fig. 4.148.

$$D_0 = \bar{Q}_0$$

Now implementing the equation of D_2, D_1, D_0 using D Flip-Flop and combinational circuit.

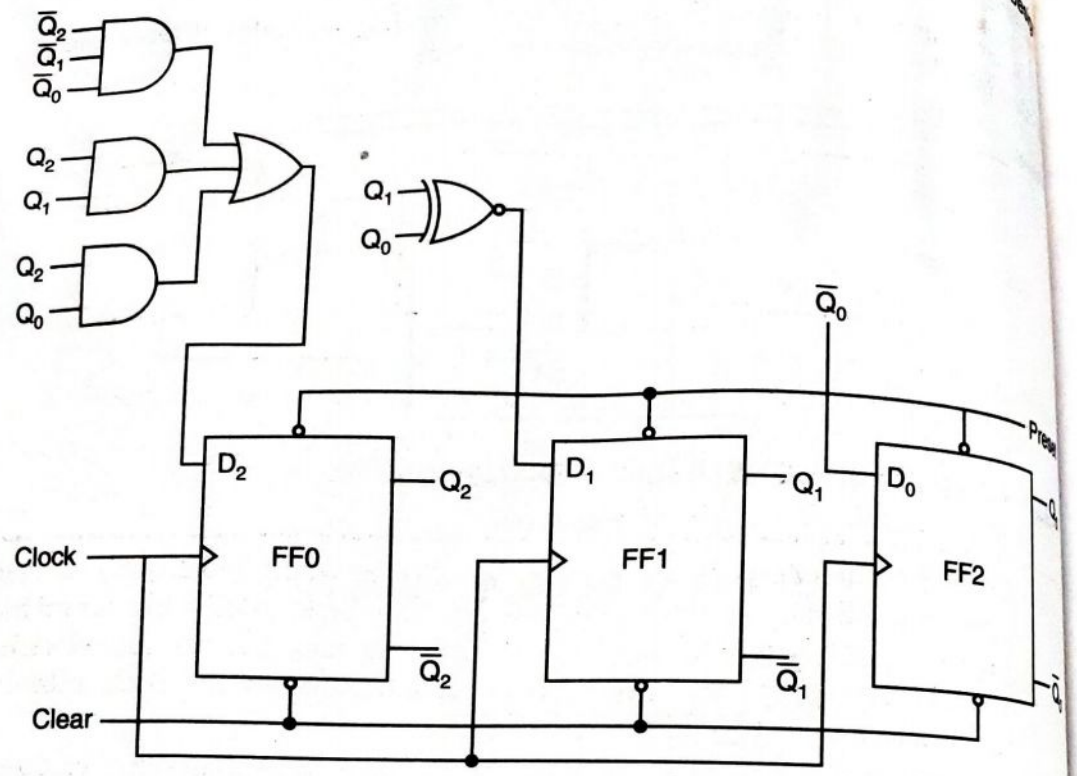


Fig. 4.149.

Multimode Counter

Multimode counter are counter which works in two or more than two mode with the help an extra input.

For example: Up/Down counter is an multimode counter which can counts in up direction as well as in down direction.

4.31.4 Asynchronous Counter and Synchronous Counter

Synchronous counter is an counter in which same clock pulse is applied to all flip-flop. In synchronous counter flip-flop are Synchronized with system clock.

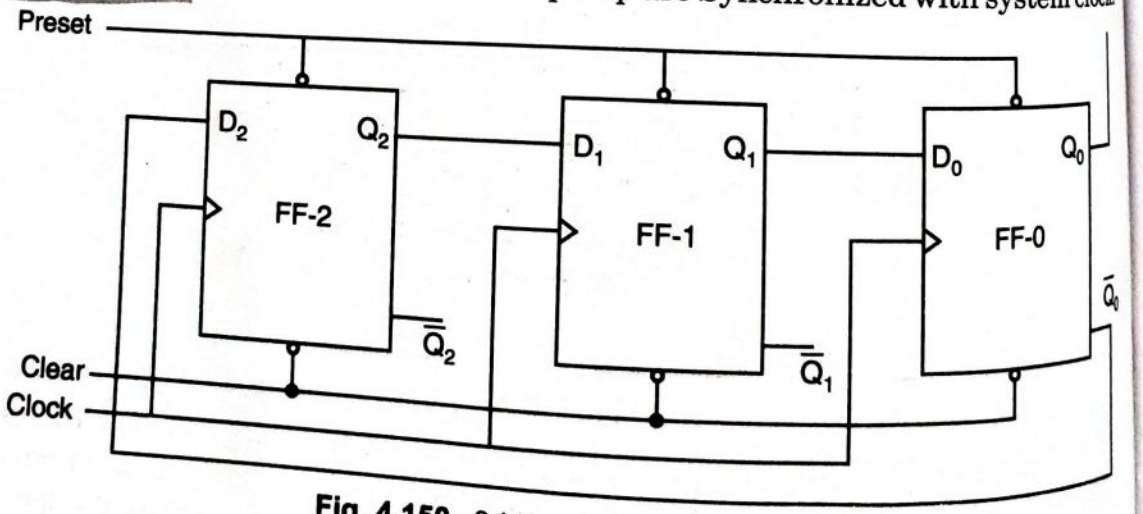


Fig. 4.150. 3-bit synchronous counter
(as same clock pulse is applied to FF_0, FF_1 & FF_2)

Synchronous Counter is an counter in which all the flip-flop are energized with same clock pulse.

In asynchronous counter the output of one flip-flop is feeded to clock input of other flip-flop which is shown in below diagram.

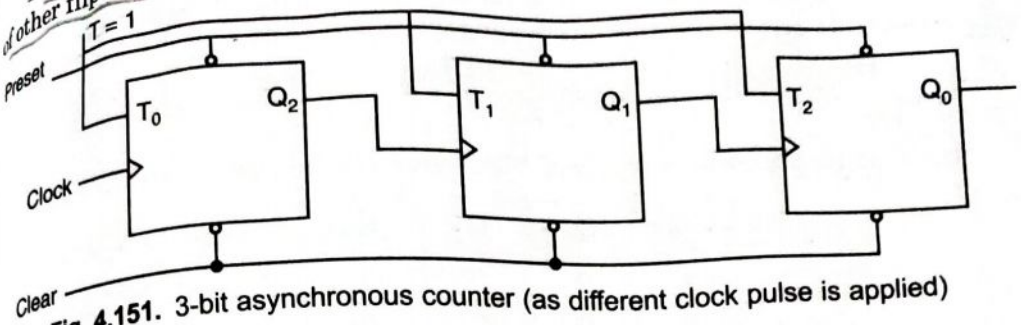


Fig. 4.151. 3-bit asynchronous counter (as different clock pulse is applied)

4.32 COMPARISON BETWEEN ASYNCHRONOUS AND SYNCHRONOUS COUNTER

- Asynchronous counter is a type of counter in which clock pulse is not common to all the flip-flops. For first flip-flop clock pulse is given and for other means 2nd flip-flop, the output of first flip-flop is acting as a clock to next flip-flop and so on while in Synchronous counter the clock pulse is common to all the flip-flops.
- Asynchronous counter (Ripple Counter) is also known as serial counter while Synchronous counter is known as parallel counter.
- Asynchronous counter (divide by N or Ripple Counter) is simpler to design while synchronous counter is difficult is to design.
- Asynchronous counter requires the least amount of hardware as compared to Synchronous Counter.
- In asynchronous counter unwanted spikes are produced which is not present in Synchronous Counter.

Asynchronous Counter/Ripple Counter

In asynchronous counter, the output of one flip flop is feeded to clock input of other flip-flop as shown in fig. 4.155.

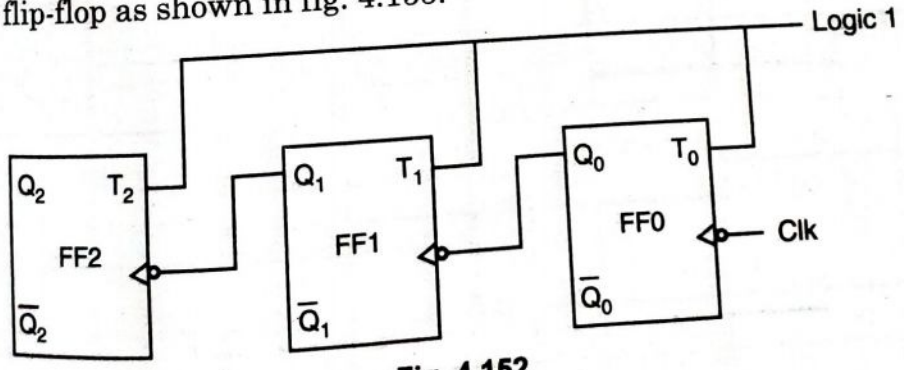


Fig. 4.152.

In this the Clk input drives FFO and output of FF0 (Q_0) drives FF1 and output of FF1 (Q_1) drives FF2 which indicates a kind of asynchronous counter. T inputs *i.e.*, T_0, T_1, T_2 are connected to logic 1. Here, each flip flop toggles at the negative edge of CLk pulse (as bubble is shown in clock pulse). As output of one flip flop (F/F) drives clock input of other, hence it is called as an **asynchronous counter** and as trigger moves like a ripple in water, hence it is

In asynchronous counter the output of one flip-flop is feeded to clock input of other flip-flop which is shown in below diagram.

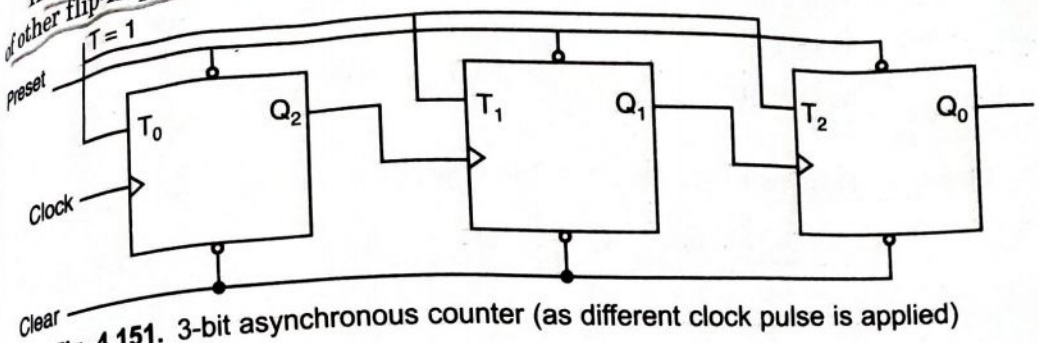


Fig. 4.151. 3-bit asynchronous counter (as different clock pulse is applied)

4.32 COMPARISON BETWEEN ASYNCHRONOUS AND SYNCHRONOUS COUNTER

- Asynchronous counter is a type of counter in which clock pulse is not common to all the flip-flops. For first flip-flop clock pulse is given and for other means 2nd flip-flop, the output of first flip-flop is acting as a clock to next flip-flop and so on while in Synchronous counter the clock pulse is common to all the flip-flops.
- Asynchronous counter (Ripple Counter) is also known as serial counter while Synchronous counter is known as parallel counter.
- Asynchronous counter (divide by N or Ripple Counter) is simpler to design while synchronous counter is difficult is to design.
- Asynchronous counter requires the least amount of hardware as compared to Synchronous Counter.
- In asynchronous counter unwanted spikes are produced which is not present in Synchronous Counter.

Asynchronous Counter/Ripple Counter

In asynchronous counter, the output of one flip flop is feeded to clock input of other flip-flop as shown in fig. 4.155.

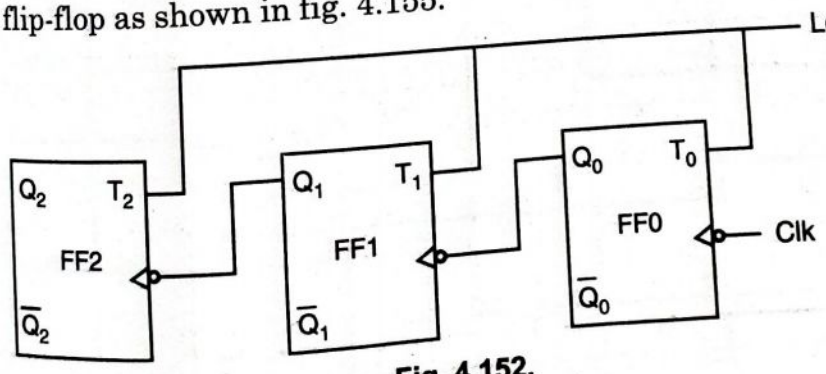


Fig. 4.152.

In this the Clk input drives FFO and output of FF0 (Q_0) drives FF1 and output of FF1 (Q_1) drives FF2 which indicates a kind of asynchronous counter. T inputs *i.e.*, T_0, T_1, T_2 are connected to logic 1. Here, each flip flop toggles at the negative edge of CLk pulse (as bubble is shown in clock pulse). As output of one flip flop (F/F) drives clock input of other, hence it is called as an **asynchronous counter** and as trigger moves like a ripple in water, hence it is

called as a ripple counter when Q_0 takes a transition from $1 \rightarrow 0$, then it c trigger FF1 means FF1 toggles and when Q1 takes a transition from $1 \rightarrow 0$ it can trigger FF2 means FF2 toggles. Hence overall propagation delay (P time is equal to sum of individual propagation delays of FF0, FF1, FF2.

$$(P.D)_{\text{Ripple counter}} = (PD)_{FF0} + (PD)_{FF1} + (PD)_{FF2}$$

Operation:

The 3-bit ripple counter truth table is given as below

Clk	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Initially all F/Fs are cleared hence $Q_2 = Q_1 = Q_0 = 0$. FF0 toggles at every clock pulses on negative transition of clock. At Ist clock pulse $0 \rightarrow 1$ transition of Q0 cannot trigger Q_1 as it's a positive change hence $Q_1 = 0$.

Similarly $0 \rightarrow 0$ state of Q_1 cannot trigger Q_2. Hence $Q_2 = 0$.

In this way counter will count from 000 – 111.

Waveform

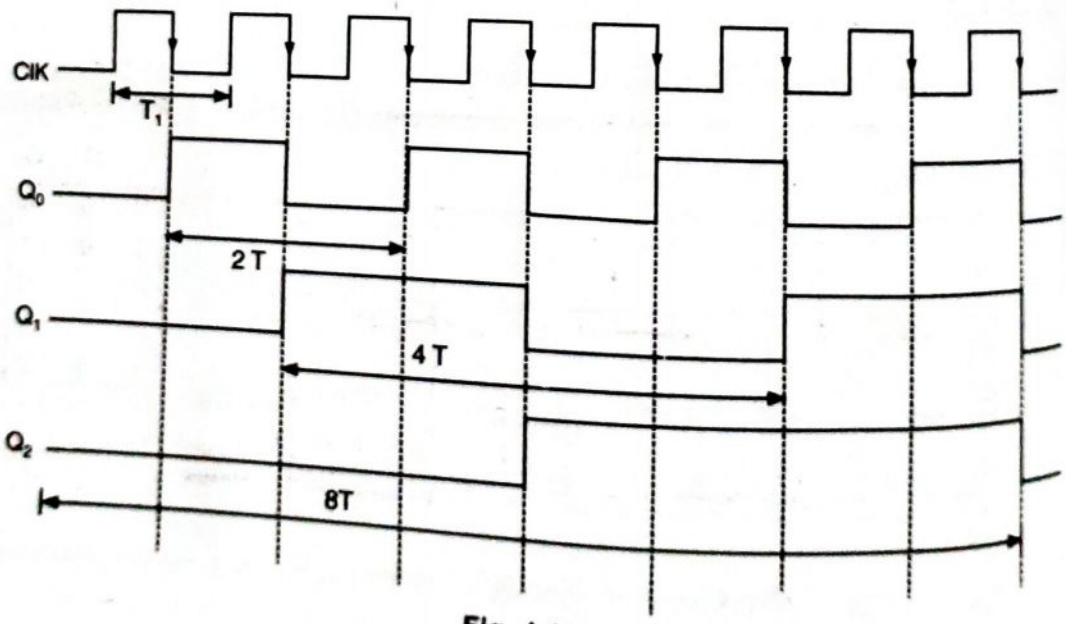


Fig. 4.153.

This counter can be utilized as a frequency counter.

As time period is becoming double, hence frequency is becoming half i.e.

$$Q_0 = \frac{1}{2}(\text{Clk f})$$

$$Q_1 = \frac{1}{4}(\text{Clk f})$$

$$Q_2 = \frac{1}{8}(\text{Clk f})$$

So by using three flip flops, we can get $2^3 = 8$ distinct/unique states. Hence it can count from $\left[0-(2^3-1)\right]$ *i.e.*, 0 – 7 states.

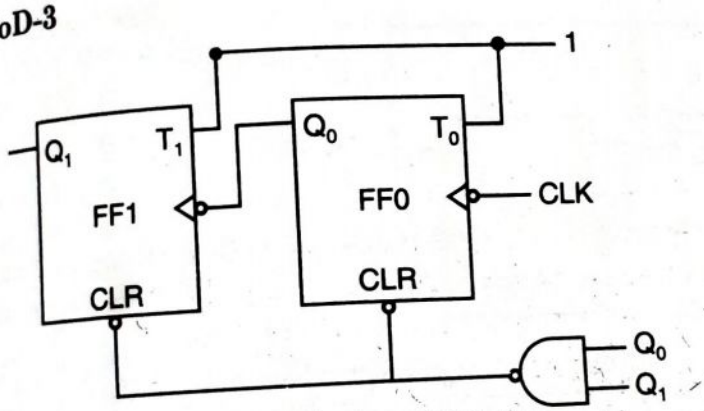
PROBLEM Design the following asynchronous (Ripple counter)

(1) MoD 3 (2) MoD 5 (3) MoD 6

(4) MoD 7 (5) MoD 9

Solution : It can be designed by specifically by J-K F/F counter. The condition J = K = 1 or by using TF/F and T = 1

(i) MoD-3

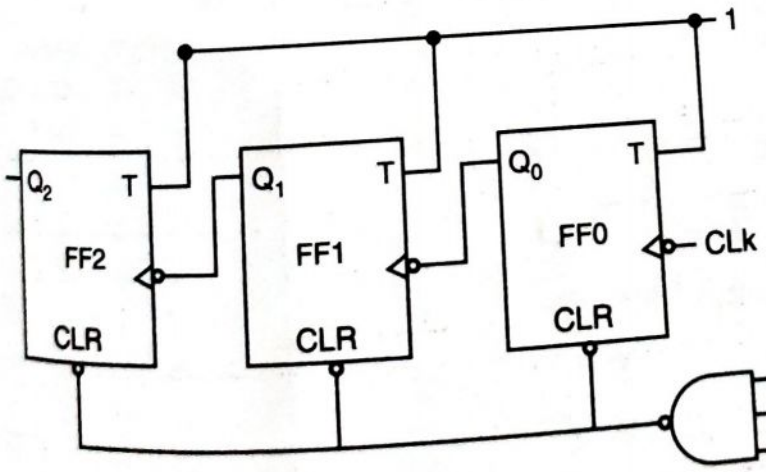


MoD-3 counts f/m

	Q_1	Q_0
0 – 2 i.e.,	0	0
	0	1
	1	0
Skipped state	1	1

Divide by 3/ MOD-3 Ripple counter

(ii) MoD-5



MoD-5 counts f/m 0 – 4 i.e.,

Q_2	Q_1	Q_1	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	Skipped states
1	1	0	
1	1	1	

Divide by 5/ MoD-5 Ripple counter