(1) Serial in, Serial out (SISO)
(2) Serial in, Parallel out (SIPO)
(3) Parallel in Serial out (PISO)
(4) Parallel in, Parallel out (PIPO)

The shift register can be designed either by J-K or D flip flop. The representation of various types of shift register is shown as follows:

(1) Serial in serial out (SISO)

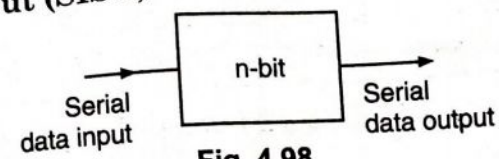


Fig. 4.98.

Here *n*-bit indicate, the data bits to be entered serial – in and data bits are outed in serial order.

(2) Serial in-Parallel out (SIPO)

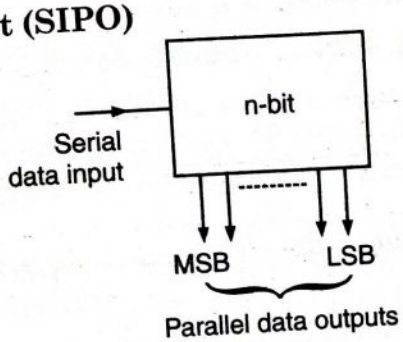


Fig 4.99.

(3) Parallel– in, Serial out

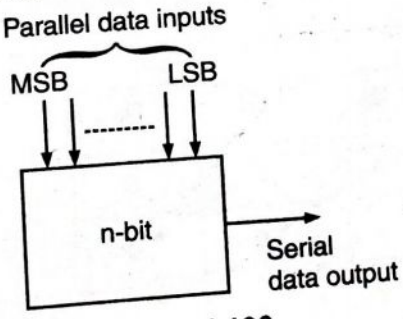


Fig. 4.100.

(4) Parallel in, parallel out

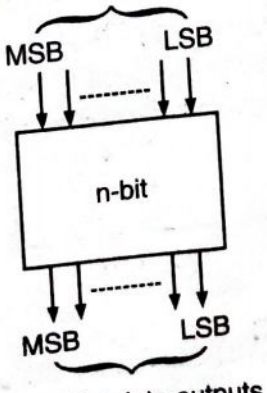


Fig. 4.101.

Let us discuss one by one all the shift register:

(1) *Serial in serial out (SISO)*-In SISO register data is entered serial i.e. data is entered one bit at a time and then next bit and data is outed and also serial, i.e. one bit at a time and then next bit at next clock pulse.

Generally one clock pulse is consumed when one bit of data is stored. The circuit using D flip flop is shown as follows:

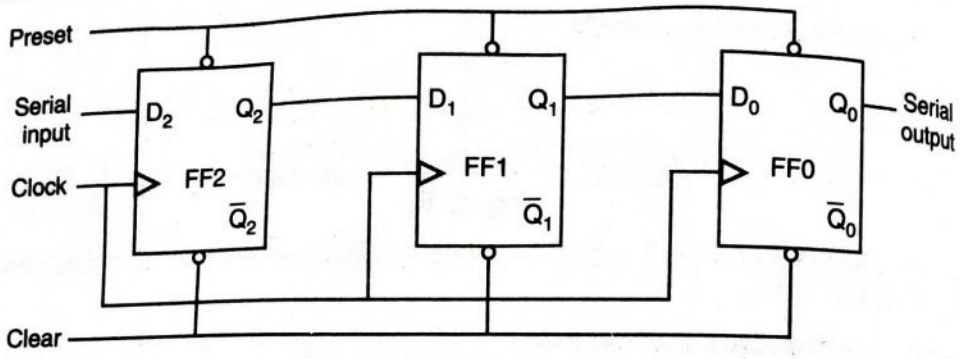


Fig. 4.102. D-type shift register (SISO)

Here we take an example of 3-bit positively edge triggered SISO register. We have the serial terminal one for input and named *serial input and other one is for output as serial output. Preset and clear are asychronous signals and used as active low signal.*

Data is entered serial but least significance bit (LSB) is stored first and then next and at last main/most significance bit (MSB) is stored.

During data output LSB is taken out firstly then next bit to LSB and at last MSB is taken out.

Suppose we want to store 101 in SISO register :

Serial In:

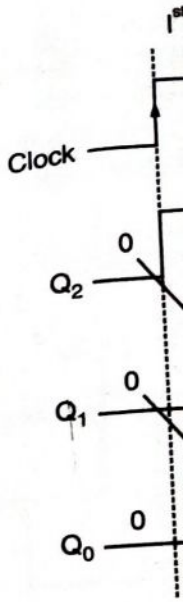
Clock	Q_2	Q_1	Q_0
Initial value	0	0	0
After Ist Clock	1	0	0
After 2nd Clock	0	1	0
After 3rd Clock	1	0	1

Value stored in 3rd clock pulse (serial IN)

Initial value stored in register is "000", when we apply '1' on D_2 (Serial input) after Ist clock pulse output Q_2 'I' and Q_1 = '0' and Q_0 = '0' because of shift in value. *Hence we need '3' clock pulse to write data in SISO* register.

Waveform

It is shown as below:



Serial out :

Clock
3rd Clock
4th Clock
5th Clock

As in third clock shifts its value to fli flip flop number '0' in next clock pulse sh takes place.

Note: Here afte data D_2 to D_1 flip flop 4th clock pulse D_2 is t vious value 'I' and taken in 5th clock pu

Waveform

We need '2' clock out hence number quired to in and out as No of clock pul Data In = 3 No. of quired in Data out = clock used = 5.

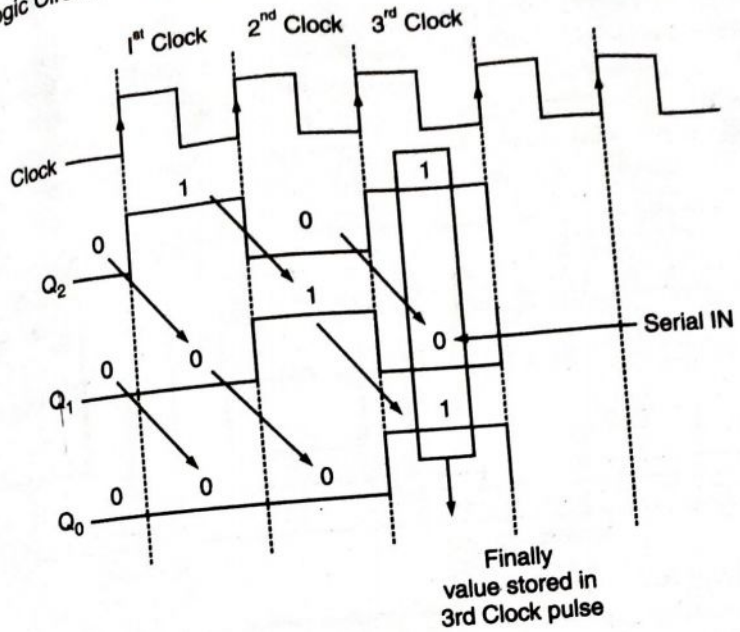


Fig. 4.103.

Serial out :

Clock	Q_2	Q_1	Q_0 (Serial output)
3rd Clock pulse	1	0	1
4th Clock pulse	1	1	0
5th Clock pulse	1	1	1

LSB (First)
Serial output
MSB (Last)

As in third clock pulse we get output '1' and flip flop number '2' gives or shifts its value to flip flop number '1' and flip flop number '1' shifts its value to flip flop number '0' and similarly in next clock pulse shifting of data takes place.

Note: Here after shifting the data D_2 to D_1 flip flop in next means 4th clock pulse D_2 is taking the previous value '1' and same value is taken in 5th clock pulse *i.e.* '1'

Waveform

We need '2' clock pulse for data out hence number of pulse required to in and out of data is given as No of clock pulse required in Data In = 3 No. of clock pulse required in Data out = 2 Total No. of clock used = 5.

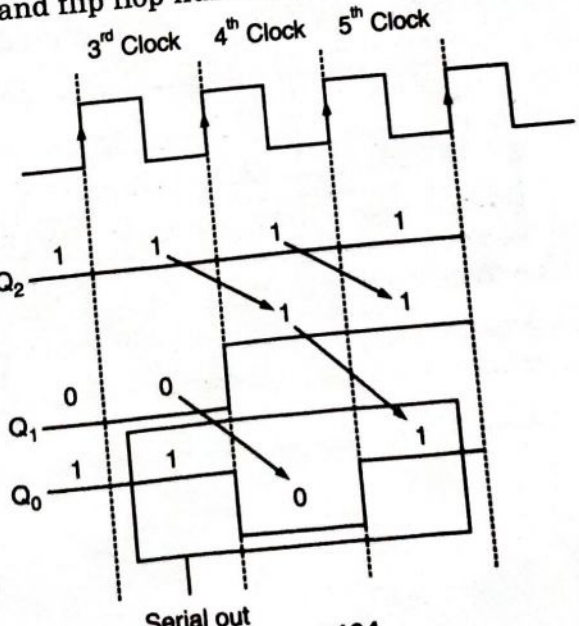


Fig. 4.104.

(2) Serial - in Parallel out (SIPO)

In serial in Parallel out (SIPO) data is entered in same style as in SISO but data bit is out in parallely means output is taken across three terminals (Q_2, Q_1, Q_0) in a single clock pulse. Once the data is stored, each bit appears on its respective output line and all the bits are available simultaneously, rather than on a bit by bit basis as with the serial output.

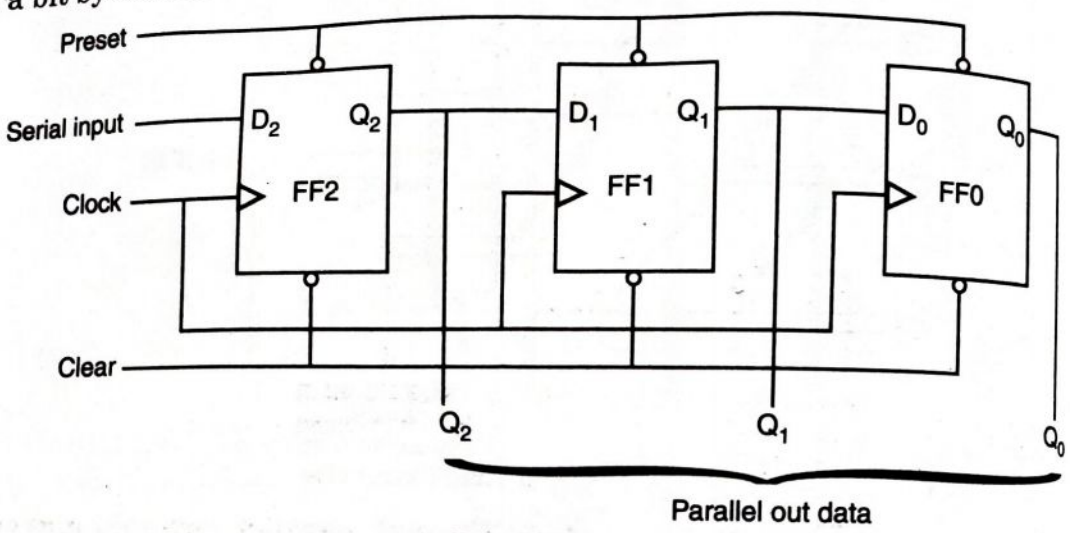


Fig. 4.105.

Serial in :

Suppose we have to entered data 011, then first bit which is feeded to serial input in LSB (Least significant bit) and at last MSB is feeded.

So first '1' bit is passed to serial input and then at first clock pulse this value is fed and stored in D_2 flip flop *i.e.* FF2. During 2nd clock pulse this value which is already stored in D_2 *i.e.* '1' is shifted to D_1 flip flop because the output Q_2 is connected to input D_1. During 2nd clock pulse '1' is fed to D_2 as serial input. During 3rd clock pulse, the value stored on D_2 *i.e.* '1' is shifted to D_1 flip flop and the value stored at D_1 flip flop is shifted to D_0 flip flop *i.e.* '1'. During this clock pulse, the D_2 is fed with next bit *i.e.* '0' and it is stored at D_2.

The table showing how data is shifted serially is given below:

Clock	Q_2	Q_1	Q_0
Initial value	0	0	0
After 1st Clock	1	0	0
After 2nd Clock	1	1	0
After 3rd Clock	0	1	1

Value stored in 3rd clock puse (Serial IN)

Wave form: The waveform of Q_2, Q_1 and Q_0 is given below:

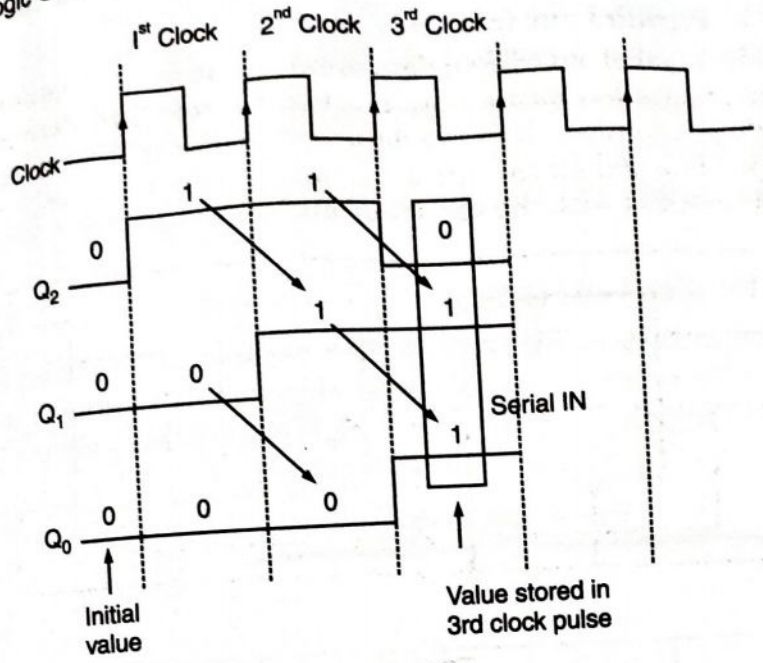


Fig. 4.106.

Parallel out: The output is taken through parallel terminal and every output is out in each flip-flop so the output is out in 3rd clock pulse.

Parallel output terminal

Clock	Q_2	Q_1	Q_0
3rd Clock	0	1	1

Waveform: The waveform for Q_2, Q_1 & Q_0 is shsown below

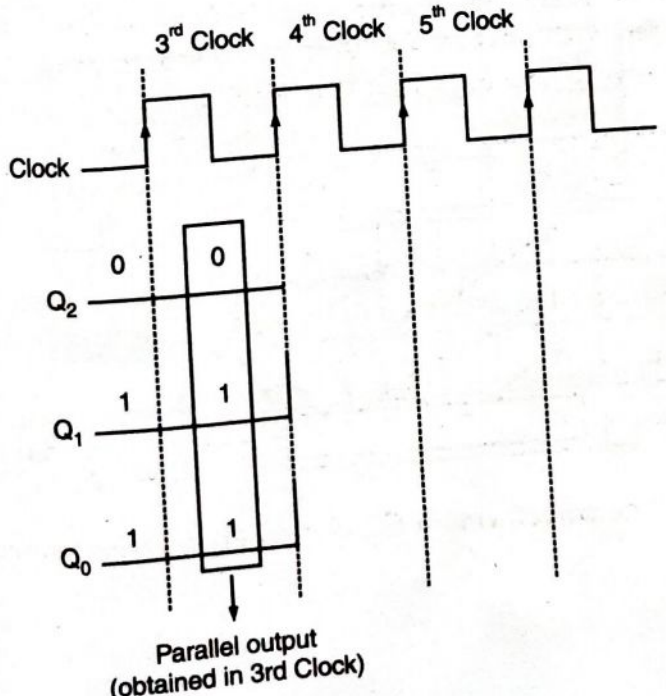


Fig. 4.107.

Total clock pulse required

No. of clock pulse required to *Data In* = 3

No. of clock pulse required to *Data out* =0

Total No. of clock pulse required = 3

Note: *This serial - IN, Parallel OUT shift register convert serial line into parallel line.*

(3) Parallel-in, serial out (PISO)

Parallel in, serial out (PISO) work as reverse of SIPO (Serial in, parallel out). In PISO data entered parallely mean if we take an example of 3-bit then input is feeded through D_2, D_1, D_0 using single clock pulse and data is out serially means one bit at a time. It is shown as below:

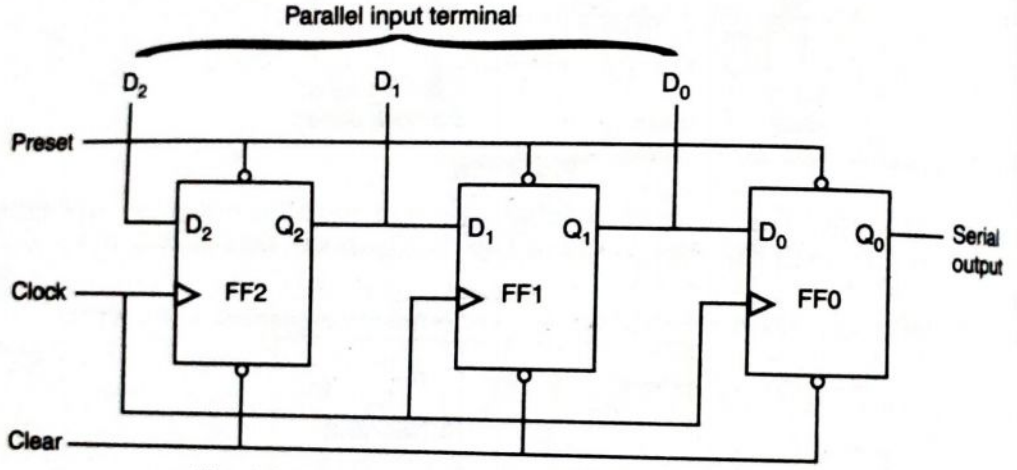


Fig. 4.108. 3-bit Parallel in Serial out Shift Register

Parallel In: Here data is entered parallely using single clock as shown in table and waveform.

Clock	D_2	D_1	D_0
Initial value	0	0	0
1st Clock	0	1	0

Suppose we have to enter 010, then we feed value to each input terminal and as soon as positive edge of clock pulse is arrived, data stored in PISO in one clock pulse.

Waveform: The waveform for D_2, D_1 & D_0 is shown below:

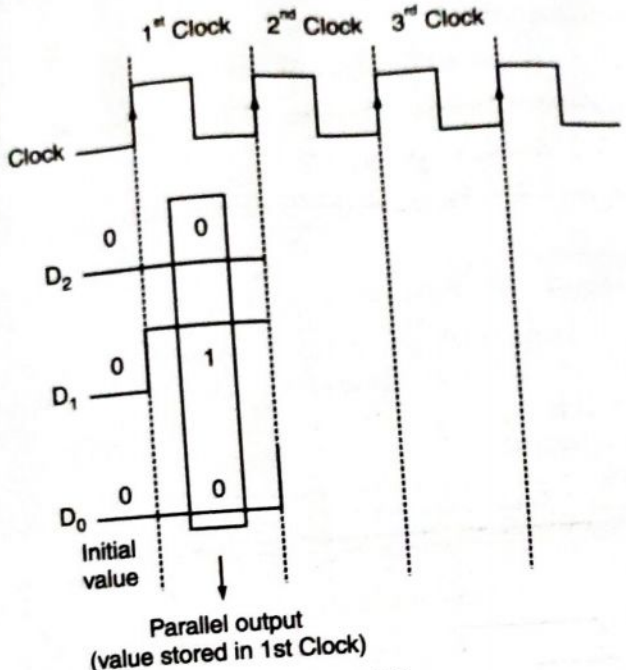


Fig. 4.109.

Serial out : In serial out, we out the data serially *i.e.* one bit in one clock pulse and hence if 3-bit register is there, then we need '3' clock pulse.

The table showing the data out in serial manner is shown below:

Clock	Q_2	Q_1	Q_0 (Serial output terminal)
			0 — LSB (First out)
2nd Clock pulse	0	1	1
3rd Clock pulse	0	0	0 — MSB (Last out)
4th Clock pulse	0	0	

Here in 2nd clock pulse, the data stored is "010" and then in 3rd clock pulse the value stored in Q_2 *i.e.* '0' is shifted to Q_1 & value stored in Q_1 is shifted to Q_0 then in 4th clock pulse the value stored in Q_2 *i.e.* '0' is shifted to Q_1 and the value stored in Q_2 i.e. '0' is shifted to Q_0. So in 4th clock pulse the value of Q_2 Q_1 Q_0 is "000". So LSB will be first out value and MSB is the last out value.

Waveform: The waveform for Q_2, Q_1 & Q_0 is given below:

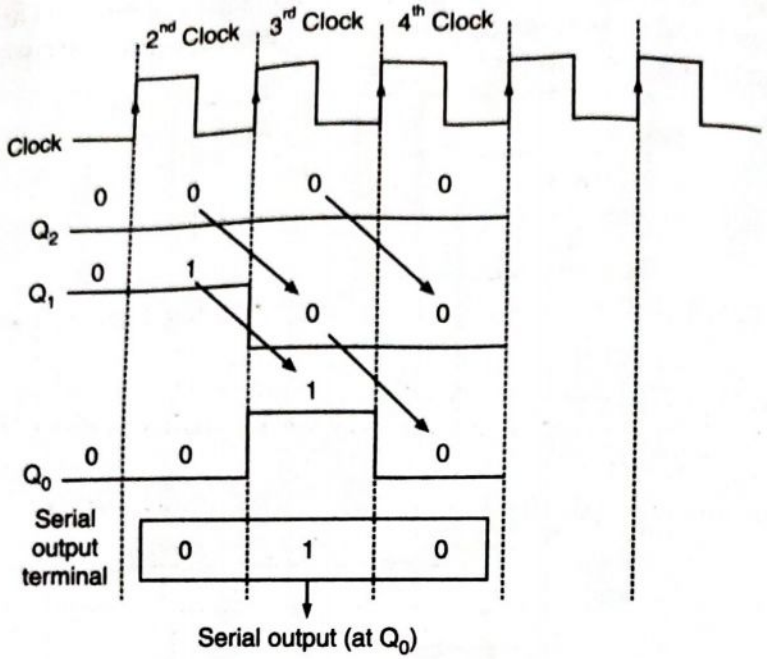


Fig. 4.110.

Totol clock pulse required:

No. of clock pulse required to *Data* in = 1

No. of clock pulse required to *Data* out = 3

Total No. of clock pulse required = Data in + Data out

= 1 + 3 = 4

Note: PISO shift register mainly convert parallel line communication to serial line communication.

(4) Parallel in Parallel out (PIPO)

In PIPO, we feed input parallely to all flip flops and also take data out parallel from all flip flops. In PIPO data entered simultaneously and data outed is also simultaneously. Here there is no interconnection between successive flip flops since no serial shifting is required. Therefore when the parallel entry of data is complete, then the respective bits will appear at the parallel outputs.

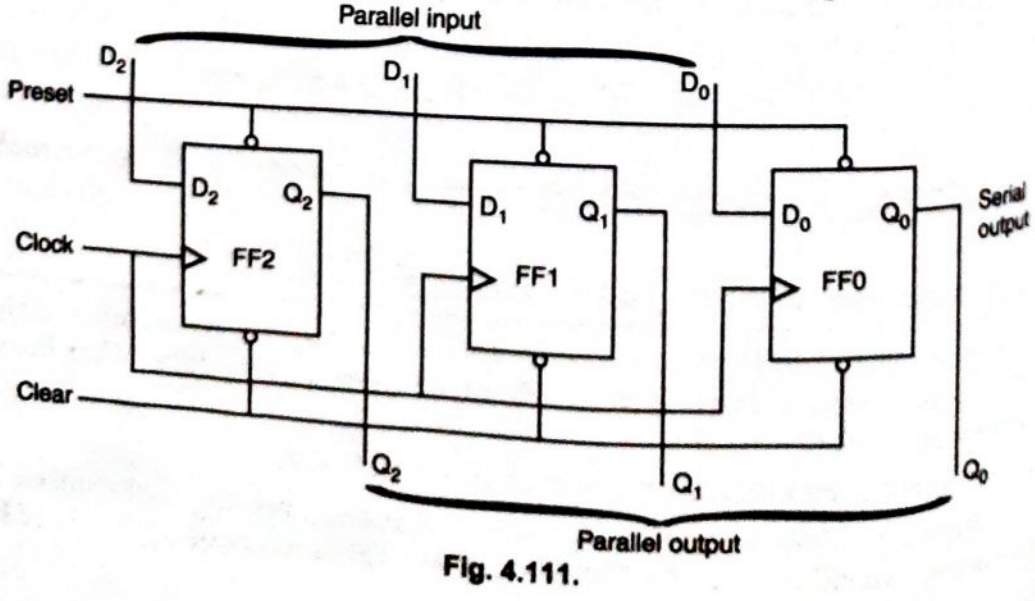


Fig. 4.111.

Parallel In: Data is entered parallel means all the value is applied to the input terminal and as soon as positive edge of Ist clock pulse arrived, the inputs value stored in the flip flop *i.e.*

Clock	D_2	D_1	D_0
Initial value	0	0	0
1st Clock	1	0	1

When **101** is fed into the flip flop, then it is fed parallely in single clock pulse.

Parallel out: The output procedure is similar to the parallel input. All the flip flop have stored binary value as soon as the positive edge of Ist clock pulse is arrived, we get output parallely.

Waveform: The waveform for D_2, D_1 & D_0 is shown below:

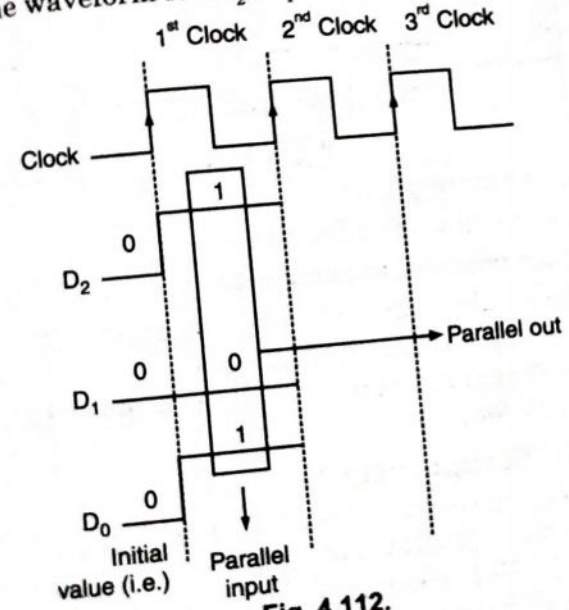


Fig. 4.112.

Total No. of clock pulse required:
No. of clock pulse required in Data in = 1
No. of clock pulse required in Data out = 0
Total No. of clock pulse consumed = Data in + Data out
= 1 + 0 = 1

Note: *As PIPO uses only two clock pulse it is fastest in shift register such as SISO, SIPO, PISO.*

4.25. 4-BIT BIDIRECTIONAL SHIFT REGISTER

A bidirectional shift register can shift data in two directions, *i.e.*, left and right. It is mostly used in those devices where we have to shift data either in right direction or left direction.

4-bit bidirectional shift register is shown in Fig. 4.113.

Working of bidirectional shift register depends upon the mode control (*M*). M passes two values *i.e.*, $M = 1$ or $M = 0$. Here, **Q_A is driving D_B input of FFB**