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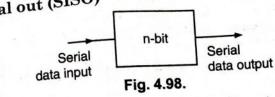
e is applied

SB)

Sequential Logic Circuits and its Design Corial in, Parallel out (SISO) (1) Serial in, Parallel out (SIPO)
(2) Serial in Serial out (DISC)

(3) parallel in Serial out (PISO)
(3) parallel in Parallel (3) parallel in, Parallel out (PIPO)
(4) parallel in parallel out (PIPO) (4) parallel III, I am be designed either by J-K or D flip flop. The representations types of shift register is shown as follows: The shift register can be designed either by J-K or D flip for of various types of shift register is shown as follows:

(1) Serial in serial out (SISO)



Here n-bit indicate, the data bits to be entered serial – in and data bits are

outed in serial order. Serial in-Parallel out (SIPO) n-bit Serial data input LSB MSB Parallel data outputs Fig 4.99.

(3) Parallel- in, Serial out

Parallel data inputs LSB MŚB n-bit Serial data output Fig. 4.100.

(4) Parallel in, parallel out

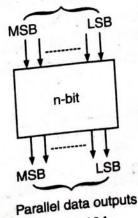


Fig. 4.101.

egister. The ccording to 306

Let us discuss one by one all the shift register:

Let us discuss one by one and (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is entered serial (1) Serial in serial out (SISO)-In SISO register data is outed as a serial (1) Serial in serial out (SISO)-In SISO register data is outed serial (1) Serial in serial out (SISO)-In SISO register data is outed serial (1) Serial in serial out (SISO)-In SISO register data is outed serial (1) Serial in serial out (SISO)-In SISO register data is outed serial (1) Serial in serial out (1) Serial in se

(1) Serial in serial out (Serial and then next bit and data is outed serial data is entered one bit at a time and then next bit at next clock pulse. serial, i.e. one bit at a time and then next bit at next clock pulse.

al, i.e. one bit at a time and all it is stored when one bit of data is stored. The Generally one clock pulse is consumed when one bit of data is stored. circuit using D flip flop is shown as follows:

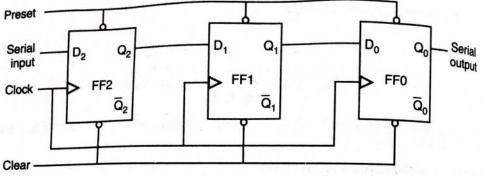


Fig. 4.102. D-type shift register (SISO)

Here we take an example of 3-bit positively edge triggered SISO register, We have the serial terminal one for input and named serial input and other one is for output as serial output. Preset and clear are asychronous signals and used as active low signal.

Data is entered serial but least significance bit (LSB) is stored first and then next and at last main/most significance bit (MSB) is stored.

During data output LSB is taken out firstly then next bit to LSB and at last MSB is taken out.

Suppose we want to store 101 in SISO register:

Serial In:

Clock	Q ₂	Q ₁	Qo	
Initial value	0	0	0	
After Ist Clock	1	0	0	
After 2 nd Clock	0	1	0	
After 3 rd Clock	1	0	1	Value stored in 3rd clock pulse (serial IN)

Initial value stored in register is "000", when we apply '1' on D_2 (Serial at) after 1st clock pulse. input) after Ist clock pulse output Q_2 'l' and Q_1 = '0' and Q_0 = '0' because of shift invalue. Hence we need '2' clock in Q_2 'l' and Q_1 = '0' and Q_0 = '0' because of shift in Q_1 = '0' and Q_2 = '0' because of shift in Q_2 in Q_2 = '0' because of shift in Q_2 in value. Hence we need '3' clock pulse to write data in SISO register.

Waveform

It is shown as below:

Sequential Logic Circuits ar Clock

Serial out:

Clock 3rd Clock 4th Clock

5th Clock

As in third clock shifts its value to fli flip flop number '0' in next clock pulse sl takes place.

Note: Here afte $\operatorname{data} D_2 \operatorname{to} D_1 \operatorname{flip} \operatorname{flop}$ $^{4^{\mathrm{th}}}$ clock pulse $\mathrm{D_2}$ is t vious value 'l' and taken in 5th clock pu

Waveform

We need '2' clock out hence number quired to in and out as No of clock pul Data In = 3 No. of quired in Data out clock used = 5.

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ered serial i.e. outed and also

is stored. The

Serial output

SISO register. t and other one gnals and used

l first and then

SB and at last

l in 3rd (serial IN)

I' on D_2 (Serial cause of shift in ter.

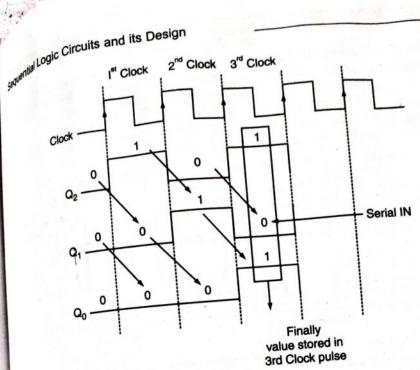


Fig. 4.103.

Serial out :

	Q ₂	Q ₁	Q ₀ (Serial output)	
Clock	-	-	TIH	LSB (First)
3 rd Clock pulse	1>	0	No.	- Serial outpu
4 th Clock pulse	1>	1	N.	MSB (Last)
5 th Clock pulse	1	1	1 11	n flop numl

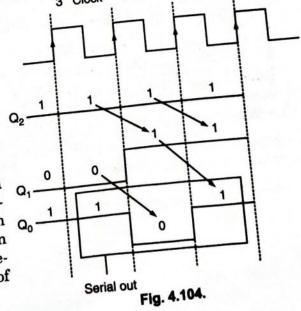
As in third clock pulse we get output 'l' and flip flop number '2' gives or shifts its value to flip flop number 'l' and flip flop number 'l' shifts its value to

flip flop number '0' and similarly in next clock pulse shifting of data takes place.

Note: Here after shifting the data D_2 to D_1 flip flop in next means declock pulse D_2 is taking the previous value '1' and same value is Q_2 taken in 5th clock pulse *i.e.* '1'

Waveform.

We need '2' clock pulse for data out hence number of pulse required to in and out of data is given as No of clock pulse required in the late of lock pulse required in Data out = 2 Total No. of clock used = 5.



(2) Serial - in Parallel out (SIPO)

Serial - in Parallel out (SIPO) data is entered in same style as in SISO In serial in Parallel out (SIPO) data is entered in same style as in SISO In serial in Parallely means output is taken across three terminals (O In serial in Parallel out (SH output is taken across three terminals (Q) data bit is out in parallely means output is taken across three terminals (Q) data bit is out in parallely means once the data is stored, each bit appears on the lock pulse. Once the data is stored, each bit appears on the lock pulse. data bit is out in parallely included at a stored, each bit appears on Q_0 in a single clock pulse. Once the data is stored, each bit appears on Q_0 in a single clock pulse. Once the data is stored, each bit appears on Q_0 in a single clock pulse. Once the data is stored, each bit appears on Q_0 in a single clock pulse. Q_0) in a single clock pulse. The bits are available simultaneously, rather than spective output line and all the bits are available simultaneously, rather than on a bit by bit basis as with the serial output.

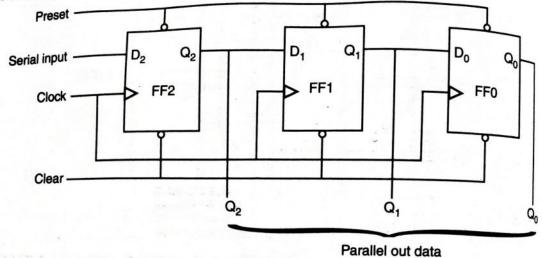


Fig. 4.105.

Serial in:

Suppose we have to entered data 011, then first bit which is feeded to serial input in LSB (Least significant bit) and at last MSB is feeded.

So first 'l' bit is passed to serial input and then at first clock pulse this value is fed and stored in D_2 flip flop i.e. FF2. During 2nd clock pulse this value which is already stored in D_2 i.e. 'l' is shifted to D_1 flip flop because the output Q_2 is connected to input D_1 . During 2nd clock pulse 'l' is fed to D_2 as serial input During 3rd clock pulse, the value stored on D_2 i.e. 'l' is shifted to D_1 flip flop and the value stored at D_1 flip flop is shifted to D_0 flip flop i.e. 'l'. During this clock pulse, the D_2 is fed with next bit *i.e.* '0' and it is stored at D_2 .

The table showing how data is shifted serially is given below:

Clock	Q ₂	Q ₁	Qo	
Initial value	0,	0	-0	
After Ist Clock	1	0	0	
After 2 nd Clock	1,	1	0	
After 3 rd Clock	10		0	
				Value stored in 3rd clock puse (Serial IN)

Wave form: The waveform of Q_2 , Q_1 and Q_0 is given below:

Sequential Logic C

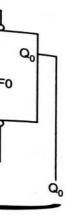
Clo

Parallel output is out i

Wavefor

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in SISO but nals (Q₂, Q₁, ars on its re. rather than



ded to serial

e this value value which output $Q_{\scriptscriptstyle 2}$ is erial input. flip flop and g this clock

ock puse

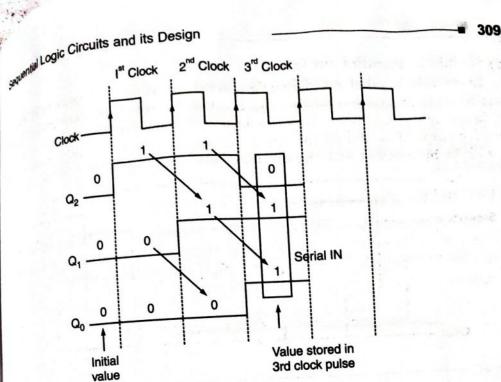


Fig. 4.106.

Parallel out: The output is taken through parallel terminal and every output is out in each flip-flop so the output is out in 3rd clock pulse.

	Parallel output terminal			
Clock	Q ₂	Q ₁	Q ₀	
3rd Clock	0,	1	: 1	

Waveform: The waveform for Q_2 , Q_1 & Q_0 is shown below

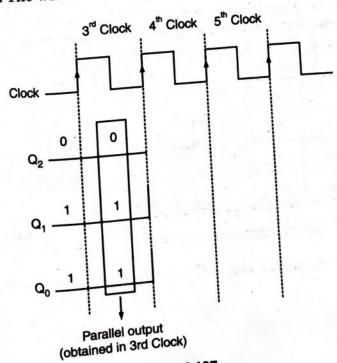


Fig. 4.107.

Total clock pulse required

No. of clock pulse required to $Data\ In = 3$

No. of clock pulse required to Data out =0

Total No. of clock pulse required = 3

Note: This serial - IN, Parallel OUT shift register convert serial line into parallel line.

(3) Parallel-in, serial out (PISO)

Parallel in, serial out (PISO) work as reverse of SIPO (Serial in, parallel parallel in, serial out (PISO) work as reverse of SIPO (Serial in, parallel parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the serial out (PISO) work as reverse of SIPO (Serial in, parallel in the series of SIPO (Serial in, parallel in, parallel in the series of SIPO (Serial in, parallel in, parallel in, parallel in, parallel in, parallel in the series of SIPO (Serial in, parallel in, out). In PISO data entered parallely mean if we take an example of 3-bit then input is feeded through D_2 , D_1 , D_0 using single clock pulse and data is out senally means one bit at a time. It is shown as below:

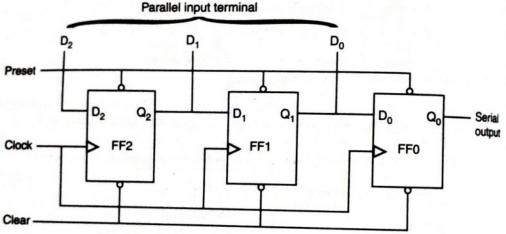


Fig. 4.108. 3-bit Parallel in Serial out Shift Register

Parallel In: Here data is entered parallely using single clock as shown in table and waveform.

Clock	D ₂	D ₁	Do
Initial value	0	0	0
1st Clock	0	1	0

Suppose we have to enter 010, then we feed value to each input terminal and as soon as positive edge of clock pulse is arrived, data stored in PISO in one

Waveform: The waveform for D_2 , D_1 & D_0 is shown below:

Sequential Logic Circuits

Clock

 D_2

D₁

Serial out: In pulse and hence if The table showi

> Clock 2nd Cloc 3rd Cloc

> > 4th Cloc

Here in 2nd close the value stored in then in 4th clock pu stored in Q_2 i.e. '0' "000". So LSB will

Waveform: T

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serial line into

rial in, parallel ole of 3-bit then data is out seri.

Serial output

ock as shown in

input terminal in PISO in one

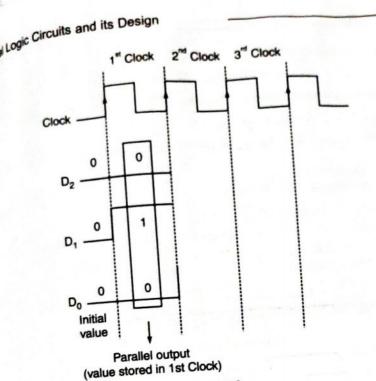


Fig. 4.109.

Serial out: In serial out, we out the data serially i.e. one bit in one clock pulse and hence if 3-bit register is there, then we need '3' clock pulse.

The table showing the data out in serial manner is shown below:

Olert	Q ₂	Q ₁	Q ₀ (Serial output terminal)	
Clock	-	+	TOH	- LSB (First out)
2 nd Clock pulse	0	1	H.H	
3 rd Clock pulse	0	0	 	MSB (Last out)
4th Clock pulse	0	0	0	· · · or

Here in 2nd clock pulse, the data stored is "010" and then in 3rd clock pulse the value stored in Q_2 i.e. '0' is shifted to Q_1 & value stored in Q_1 is shifted to Q_0 then in 4th along then in 4^{th} clock pulse the value stored in Q_2 i.e. '0' is shifted to Q_1 and the value stored in Q_2 i.e. '0' is shifted to Q_1 and the value of Q_2 Q_1 is When Q_2 i.e. '0' is shifted to Q_0 . So in 4^{th} clock pulse the value of Q_2 Q_1 Q_0 is '00' So I CD. So LSB will be first out value and MSB is the last out value.

Waveform: The waveform for Q_2 , Q_1 & Q_0 is given below:

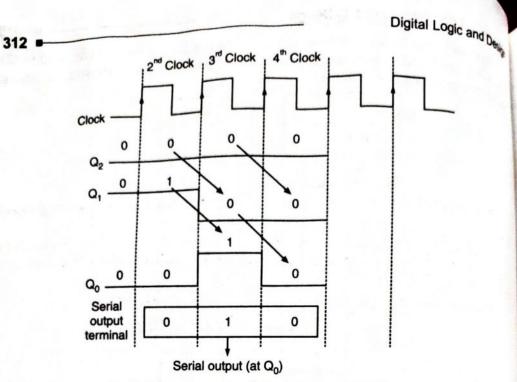


Fig. 4.110.

Totol clock pulse required:

No. of clock pulse required to Data in = 1

No. of clock pulse required to Data out = 3

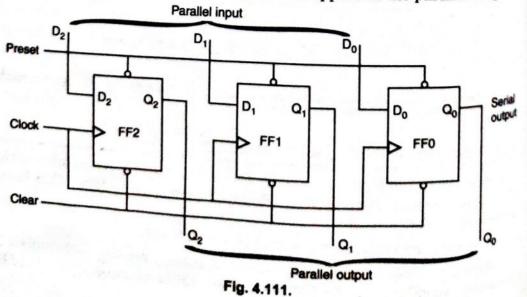
Total No. of clock pulse required = Data in + Data out

$$= 1 + 3 = 4$$

Note: PISO shift register mainly convert parallel line communication to serial line communication.

(4) Parallel in Parallel out (PIPO)

In PIPO, we feed input parallely to all flip flops and also take data out parallel from all flip flops. In PIPO data entered simultaneously and data outed is also simultaneously. Here there is no interconnection between successive fig. flops since no serial shifting is required. Therefore when the parallel entry of data is complete, then the respective bits will appear at the parallel outputs.



Sequential Logic Circuits Parallel In: Dat input terminal and a input stored in the flyalue stored in the fly

When 101 is fe

Parallel out: flip flop have store is arrived, we get o Waveform: Th

> Total No. of No. of clock No. of clock Total No. of

Note: As Pl SISO, SIPO, PI

4.25. 4-BIT BIC

A bidirectional It is mostly use direction or lef 4-bit bidire

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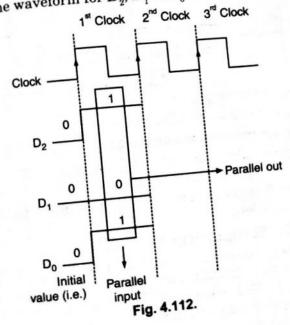
Logic Circuits and its Design Parellel In: Data is entered parallel means all the value is applied to the parellel and as soon as positive edge of Ist clock pulse arrived the single flow i.e. parallel In: Data is entered parallel means all the value is applied to the parallel means all the value is applied to

nal and as sold in the flip flop i.e.	D ₂	D ₁	Do
Clock Initial value	0	0	0
1" Clock	1	0	1

When 101 is fed into the flip flop, then it is fed parallely in single clock

parallel out: The output procedure is similar to the parallel input. All the parallel out. The occurre is similar to the parallel input. All the parallel binary value as soon as the positive edge of Ist clock pulse we get output parallely. garrived, we get output parallely.

Waveform: The waveform for D_2 , D_1 & D_6 is shown below:



Total No. of clock pulse required:

No. of clock pulse required in Data in = 1

No. of clock pulse required in Data out = 0 Total No. of clock pulse consumed = Data in + Data out

Note: As PIPO uses only two clock pulse it is fastest in shift register such as SISO, SIPO, PISO.

125. 4-BIT BIDIRECTIONAL SHIFT REGISTER Abidirectional shift register can shift data in two directions, i.e., left and right. It is mostly used in those devices where we have to shift data either in right

direction or left direction.

4-bit bidirectional shift register is shown in Fig. 4.113.

Working of bidirectional shift register depends upon the mode control (M). We working of bidirectional shift register depends of D_B input of FFB asses two values i.e., M = 1 or M = 0. Here, Q_A is driving D_B input of FFB

nication to

ce data out data outed cessive flip llel entry of l outputs.

> Serial output

Q₀