

4.21. REGISTER

It is a group of flip flops and is used for storing binary information. Flip-flop stores one bit of information and is called as binary cell or 1-bit memory is called as binary cell or 1-bit memory cell. In this way—

"An 'n' bit register is basically a group of a n-flip-flops and is capable of storing n-bit information.

Applications of register

It is used in memories

Used in microprocesors.

Register can be classified into two categories

Register Memory register Shift register

Memory Register

A register that is used to store binary information is known as memory register.

Shift Register

A register that is used to shift binary information either to right or to the left is called as shift register."

Shift Register

Shift Register is a type of Sequential circuit (means which has memory) that is formed by combination of flip flops and is capable of shifting data from left to right or right to left.

Shift register performs two basic functions

(i) Shifting of Data (Transfer of Data)

(ii) Storage function

Shifting of Data

It is defined as the movement of data from stage to stage (left to right or right to left) within the register or into or out of the register upon the applica-

Storage Function

It is defined as the number of bits (1's or 0's) of digital data it can retain. The storage function will depends upon the number of flip flops which are connected to form register and if the to form register e.g. if three flip flops are connected together, then register is capable of storing 2 his are connected together, then register is capable of storing 3-bits. So we can say that if 'N' flip flops are there, then it can store 'N' bits. Due to the storing a bet store 'N' bits. Due to this storage feature, it is an important memory device. Let us take an e.g. showing the concept of storage feature:

Sequential Logic Circu Case I. When

input and clock p stores the 'l' and he be set. When 'l' on the flip flop will re storing the 'l'. It is

So when D = 0I' bit is stored wh mains a 'l' if alrea Case II When

the input and clock stores the '0' and to be in Reset stat put is removed, mains in the Rese bit. It is shown as

So when D ='0' bit is stored w mains a '0' if alre

BASIC CO 4.22

It deals with the

Shift Registe digital system. process of mover The classification

- (i) Serial s
- (iii) Parallel
- (v) Rotate Generally s
- Serial s
- Paralle

Serial shi clock pulse e.g.

Parallel s are there, there pulse.

Various d

(i) Serial Shi

Here if we means the mo rection as sho

Here arro ment (serial o are used to in Logic and Design

ation.] Flip-flop bit memory is

d is capable of

n as memory

right or to the

has memory) ing data from

ft to right or the applica-

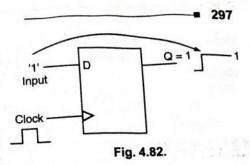
n retain. The re connected en register is e, then it can y device. Let

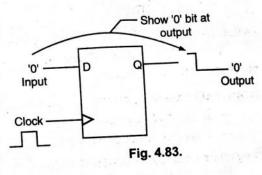
Sequential Logic Circuits and its Design Care I. When I' bit is applied to the Case I clock pulse is applied that and clock pulse is applied that and hence flip flop is so input and rand hence flip flop is said to when I' on the input is remainded. when I' on the input is removed, will remains in the set He set. Will remains in the set state, the flip flop will remains as helow the flip nor n'. It is shown as below:

ring the D = 1, then Q = 1 means bit is stored when clock occurs or re-Tour 18 of if already in that state.

Case II When '0' bit is applied to heinput and clock pulse is applied that the input of and hence flip flop is said obe in Reset state. When '0' on the input is removed, the flip flop will repains in the Reset state, storing the '0' hit. It is shown as below:

 S_0 when D = 0, then Q = 0 means V bit is stored when clock occurs or remains a '0' if already in that state.





4.22 BASIC CONCEPTS

It deals with the functions performed by the shift Register.

Shift Register are commonly used for temporary storage of data with in the digital system. Registers are formed by flip flops. The shifting of data is the process of movement of bits into or out of the register with the help of clock input. The classification of data shifting are:

- (i) Serial shift right
- (iii) Parallel shift in
- (v) Rotate right
- (ii) Serial shift left
- (iv) Parallel shift out
- l(vi) Rotate left.

Generally shifting involves two process i.e.

- Serial shift

Serial shift means bits are transferred/shifted one by one according to clock pulse e.g. for four bits, '4' clock pulses are required to shift.

Parallel shift means bits are transferred simultaneous means if '4' bits are there, then '4' bits are transferred at the same time and in single clock Pulse.

Various data Shifting Methods

(i) Serial Shift Right

Here if we have '3' bits, then right shift means the movement of data in right direction as shown in figure 4.84 (a).

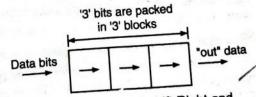


Fig. 4.84. (a) Serial shift Right and than out

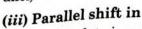
ment (serial or parallel) the movement of bits in right direction, the '3' blocks Here arrows indicate type of moveare used to indicate '3' bits.

(ii) Serial Shift Left

Here if were have '3' bits, then shift left means the movement of data in left direction as shown in figure 4.85 (b).

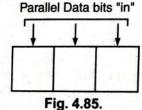
'3' bits are packed in '3' blocks. Here the arrow indicate the direction and type of data movement (serial or par-

allel)



Here the data is entered parallelly means simultaneously. It is represented as in figure 4.85.

Data "out"



Here '3' bits are entered in parallel order.

(iv) Parallel shift out

Here the data bits are out in parallel mode. It is shown as follows:

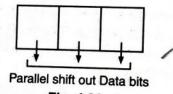


Fig. 4.86.

Here '3' bits are out in parallel mode. The arrow indicate the direction and type of data movement.

(v) Rotate right

Here the data bits are shifted in right direction and keeps on circulating as shown in figure 4.71.

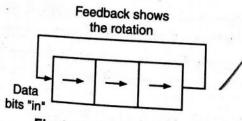


Fig 4.87. Rotate right

Here the feedback is used to rotate the bits and the arrow indicate the direction of movement.

Here the data bits are shifted in left direction bits "in" and keeps on circulating as shown in fig.

Here the feedback is used to rotate the bits in left direction and arrows are used to indicate the direction of movement.

Digital Logic and Design '3' bits are packed in '3' blocks

Feedback shows

the rotation

Fig. 4.84. (b) Serial shift left and then out

Sequential Logic Circuit 4.23 SHIFT LEFT AN These concepts are u

Shift Left

Here the data bit the left direction. follows:

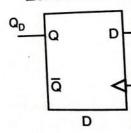
Here the '3' bits direction as shown

Left us take an _{left,} then in first cl Then in next (s

Then in third o So, we can sa bits if it is serial significant bit (I

4.23.1. Shift Le

Shift left regis Let us draw t



Here '4' D fli '4' bits. Suppose most bit. '0' bit storing '0' bit me '0'/or flip flop A connected to $Q_{_{\mathrm{A}}}$

When the s flop A and the number is now ^{applied}. Then a flip flop is shift flop C. The last pulse is applied shifted to 'B' fli the '0' stored in shift left is car gic and D_{esign}

Data bits nift left and

represented

ows:

lirection and

irculating as

ck shows otation Rotate left d arrows are

Logic Circuits and its Design

LEFT AND SHIFT RIGHT CONCEPTS

113 SHIFT LEFT AND SHIFT RIGHT CONCEPTS these concepts are used for shifting the data into the register.

Here the data bits are shifted into Data bits out Here into left direction. It is shown as Here the '3' bits are shifted in left

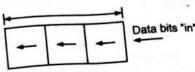


Fig. 4.89. Shift left

irection as shown by arrow. (MSB)

 D_1 D_0 means '3' bits i.e. 110 are shifted in Left us take an e.g. 1.0 D_2 then in first clock cycle ' C_1 ', D_0 is passed i.e. 'O' is fed i.e. $D_0 = 0$

Then in next (second) clock cycle ' C_2 ', D_1 is fed into the flip flop i.e. $D_1 = 1$ Then in third clock cycle ' C_3 ', D_2 is fed into flip flop i.e., $D_2 = 1$.

So, we can say that '3' clock pulses are required to fed the '3' data bits if it is serial shift left and data should be outered or 'in' from least significant bit (LSB or D_0 as in example).

4.23.1. Shift Left Register Circuit

Shift left register can be formed using D and JK flip flop. Let us draw the shift left register using D flip flop first, i.e.

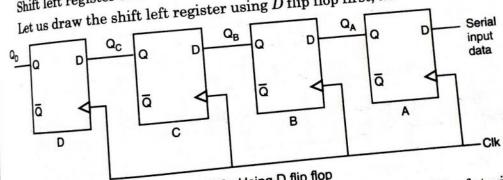


Fig. 4.90. Using D flip flop

Here '4' D flip flops are connected together and hence it is capable of storing 4 bits. Suppose we want to pass 1100 into the register, it begins with right most bit, '0' bit is applied to serial input data, then flip flop A is reset, thus storing '0' bit means Q_A is '0'. Next '0' is applied to the serial input, making $D = \emptyset$ or fin for R is When the flip flop B is where Q_A is Q_A is connected to Q_A output.

When the second clock pulse occurs, the '0' data input is shifted to the flip lop A and the '0' in the flip flop A is shifted to flip flop B. The '0' in the binary number is now applied at the serial input line and the third clock pulse is now applied at the serial input line and the flip flop A and the '0' stored in applied. Then at third clock pulse 'l' is applied at flip flop A and the '0' stored in flip flop is a life flow in the 'O' stored in flip flop B is shifted to flip flip flop is shifted to flip flop B and the '0' stored in flip flop B is shifted to flip flop C. The stored in flip flop B and fourth clock lop C. The last bit i.e. '1' is now applied at the serial input line and fourth clock pulse is an arrived to flip flop and the '1' stored in A flip flop is pulse is applied. This '1' enters into A flip flop and the '1' stored in A flip flop is shifted to C flip flop and shifted to 'B' flip flop and the 'O' stored in 'B' flip flop is shifted to C flip flop and the 'O' stored in 'B' flip flop. Thus entry of '4' data bits in the '0' stored in B inp nop is similar to B' flip flop and the '0' stored in B inp nop is similar to B' flip flop and the '0' stored in C flip-flop is shifted to D flip flop. Thus entry of '4' data bits in shift left: shift left is carried out.

Operation of shift – Left Register

	QD	Q _C	QB	QA	Serial output at (
Initial value	0	0	0	0	0
I st Clock pulse	0	100	10 1	_0	0
2 nd Clock pulse	0	0	_0 ^	/0	0
3 rd Clock pulse	0	_0 ^	/0 / /	1	0
t th Clock pulse	0	0	1	1	0

The timing diagram or waveform is as shown below.

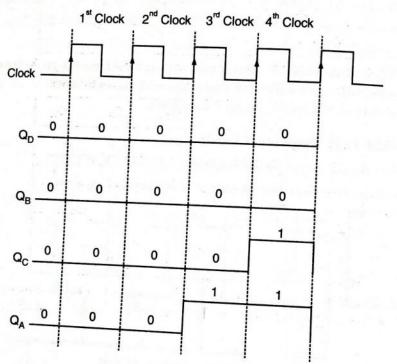


Fig. 4.91.

The designing of serial left register using JK flip flop is shown as follows:

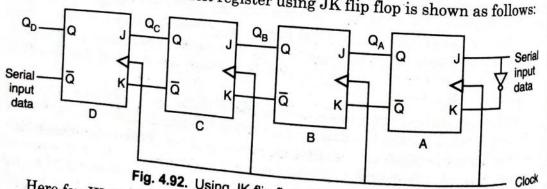


Fig. 4.92. Using JK flip flop shift left register Here for JK flip flop, it require connection to both J-K inputs. Input data connected to the Jand K: are connected to the J and K in puts of the right most (LSB) of flip flop. In order to input 1, the inputs of J-1 8 To of the right most (LSB) and K in puts and to input 1', the inputs at J=1 & K=0 (as NOT gate is connected to K input) and

Sequential Logic Circuits a for input '0', J = '0' & K for input will be shifted the data will be e.g. If all stages ar connected to stage A. T the logical- 1 input en shift pulses as showing

> Initial Ist Clo 2nd CI 3rd Cl

> > 4th Cl

In case 2, the sh all stages are set i.e.

> Initia Ist CI 2nd (

In case 3, consi more shift pulses b below:

Ini St 2ⁿ 3" 4

Note: In order (LSB) i.e. A is LSF

4.23.2. Shift Rig

Here the data into the right dire as follows:

Logic Circuits and its Design

snould be applie shifted bit by bit to the left. will be sufficient and steady '1' is applied at the serial input data is a stage A. The data after four shift pulses are given as follows: fall stages are reset and steady '1' is applied at the serial input data age. If all stage A. The data after four shift pulses are given as follows. Here to stage A & then shifts left to stage D of the to stage A. The usual arcer four shift pulses are given as follows. Here imported 1 input enters into stage A & then shifts left to stage D after four includes as showing. the logues as showing.

wing.	QD	Q_{C}	Q_B	QA
nitial value	0	0	0	0
st Clock pulse	-0	0	0	1
2 nd Clock pulse	0	100	11	1
3 rd Clock pulse	0 *	11	11	/
4th Clock nulse	1	te 0 and	1-	

In case 2, the shifting of alternate 0 and 1 data into stage A, starting with stages are set i.e. 1111. These stages are shown as follows:

i.e. 1111. Thes	Q _D	Q _C	Q _B	Q _A
nitial value	1	/1	1	1
l st Clock pulse	1	11	1	1
2 nd Clock pulse	1 2	1-	10	/0
3 rd Clock pulse	12	0-	0 1	/
4 th Clock pulse	0	1	shown i	n tabl

In case 3, consider starting with 0110 as shown in table and applying four more shift pulses but placing logical 'O' at serial input to stage A as shown below:

	Q _D	Q _C	Q_B	Q _A
1 1 1 1 1 1	-	1	1	0
Initial value	0		.0	_0
Ist Clock pulse	1	1	100	10
2 nd Clock pulse	12	100	100	0
3 rd Clock pulse	0	10	0 *	0
4 th Clock pulse	0		us start	with le

Note: In order to shift the bits, it always start with least significant bit (SB) i.e. A is LSB & D is MSB in the particular example.

4.23.2. Shift Right

Here the data bits are shifted the right direction. It is shown 8 follows:

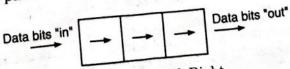


Fig. 4.93. Shift Right

follows:

and Design

Serial input data

Clock

iput data . In order nput) and 302

Here the three bits are shifted in right direction as shown in fig. (by the latter than the constant D_2 and D_3 are shifted in right direction as shown in fig. (by the latter than the constant D_2 and D_3 are the constant D_3 and D_4 are the constant D_4 and D_5 are the constant D_4 and D_5 are the constant D_5 and D_6 are the constant D_5 and D_6 are the constant D_6 are the constant D_6 are the constant D_6 and D_6 are the constant D_6 and D_6 are the constant D_6 are the co Here the three bits are shifted in the sample i.e. $D_2 D_1 D_0$. Here in first clock cycle, arrows). Let us take an example i.e. $D_2 D_1 D_0$. D_2 is fed i.e. $D_2 = 1$

In second clock cycle, the D_1 is fed i.e., $D_1 = 0$.

Then in third clock cycle, the D_0 is fed i.e. $D_0 = 1$

Then in third clock cycle, the cycle, then in third clock cycle, the cycle, then in third clock cycle, then in third clock cycle, the cycle, then in third clock cycle, then in third c So, we can say that d_{ata} should be entered or "in" through bits if it is serial shift right and data should be entered or "in" through MSB (Most significant bit i.e. D_2).

Shift Right Circuit

It can be formed using D or JK flip flop. The circuit formed using D flip $f_{\mathbb{Q}_p}$ is shown below:

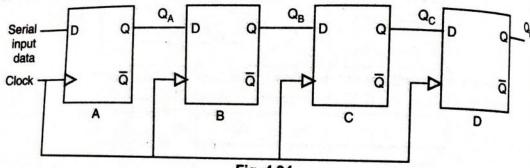


Fig. 4.94.

In this shift register, the least significant bit (LSB) of Data input is fed first means least significant bit (LSB) acts as serial Input data. The clock pulse is applied to all the flip flop simultaneously.

Let us take an e.g. i.e. 1011 is passed, then LSB bit i.e. '1' is passed to serial input data & at 'A' flip flop, this bit 'l' is passed to D and at first clock pulse, flip flop A is set, thus storing the 'l'. Then next bit i.e. 'l' is applied to serial input making D=1 for flip flop A & D=1 for flip flop B because the input of B flip flop is connected to Q_A output.

When the second clock pulse arrives, the 'l' on the data input is shifted to the flip flop A & then 'l' on A is shifted to B and '0' bit is applied at data input and the third clock pulse is now applied. The '0' is entered in flip flop A & the " stored in 'A' is shifted to B and the value stored on B i.e. 'I' is shifted to 'C' flip flop. Then fourth clock pulse is applied and 'l' bit is passed to data input and the '0' stored in flip flop A is now shifted to B and the 'l' stored in flip flop B is nowshifted to flip flop C and the 'l' stored in 'C' is shifted to 'D' flip flop.

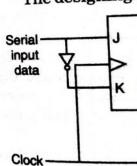
The operation is given as follows:

Initial	Q _A	QB	Qc	Q _D	Serial output at Q
Initial value I st Clock pulse	0	0	0	0	0
2 nd Clock pulse	1	0	0	0	0
3rd Clock pulse	1	1	10	0	0
4 th Clock pulse	0	1	1	~0	0
		-0	1	1	1

Sequential Logic Circuits Waveform : The the waveform of outp

Clock

The designing



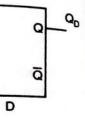
Here the data Kinputs. In order $^{\prime 0^{\prime}}$, the value of $m{J}$

The truth tak

The truth ta tially reset shift gic and Design ig. (by using ock cycle, the

the '3' data n" through

 $\log D$ flip flop



ut is fed first lock pulse is

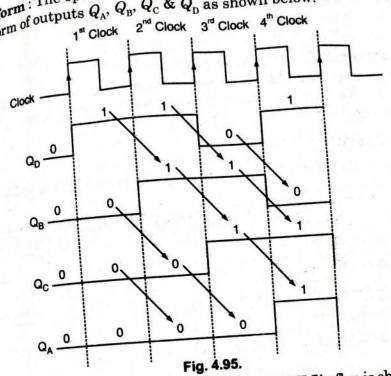
sed to serial ck pulse, flip serial input of B flip flop

is shifted to t data input op A & the T ted to 'C' flip nput and the lop B is now

ut at QD

Sequential Logic Circuits and its Design The operation is shown in the table, from there we can draw waveform of outputs Q_A , Q_B , Q_C & Q_D as shown below: Waveform of outputs Q_A , Q_B , Q_C & Q_D as shown below:

1st Clock 2nd Clock 2nd Clock 3nd Clock 1st Clock 2nd Clock



The designing of the serial right register using J-K flip flop is shown as below:

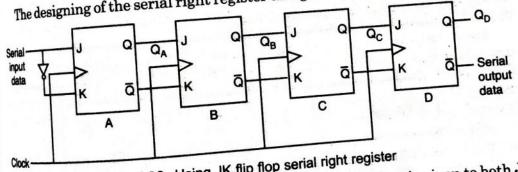


Fig. 4.96. Using JK flip flop serial right register

Here the data is entered from the LSB bit. The data input is given to both J-Kinputs. In order to pass input 1, the J=1 & K=0 is passed and to pass input 1 the J=1

The truth table showing the data input 1101 is given as below: V, the value of J = 0 and Ks = 1.

le showing the		QB	Qc	QD
	QA	0.	0	0
Initial value	0>	0	0.	0
I st Clock pulse	1>	0	0	0
2 nd Clock pulse	0>	1	1	0
3 rd Clock pulse	1>	-0	10	1
4th Clock pulse	1		0: 011 1	٠.,

The truth table showing the action of shifting all logical - 1 inputs into inihally reset shift register as below:

			-	
	Q _A	Q _B	Q _C	QD
Initial value	0	0	0	0
I st Clock pulse	1	0	0	0
2 nd Clock pulse	0	1	0	_0
3 rd Clock pulse	1	0	1	~ 0
4 th Clock pulse	1	1	0	1

Suppose we want to pass 1011 to JK base shift right shift register, the truth table is shown as follows:

	$Q_A(LSB)$	$Q_{\scriptscriptstyle B}$	Q_c	Q_D (MSB)
Initial condition	0	0	0	0
Ist clock pulse	- 1	0	0	0
2nd clock pulse	1	1	0	0
3rd clock pulse	0	1	1	0
4th clock pulse	1	0	1	1

Here when 1011 is applied at J then K is 0100 because NOT gate is applied to K.

So, the waveform is shown as below.

	Q _A	Q_B	Q _C	Q_D
Initial value	0	0	0	0
I st Clock pulse	1	0	10	10
2 nd Clock pulse	1	1	10	\ 0
3 rd Clock pulse	1	1	1	0
4 th Clock pulse	1	1	1	1

Fig. 4.97.

4.24 TYPES OF SHIFT REGISTER

In shift register the data is shifted in and shifted out from the register. The shifting process involved to the shifted in and shifted out from the register. shifting process involved to two process i.e. Serial or parallel shift. According to these combination shift register are of following types:

Sequential Logic Circuits and (1) Serial in, Serial o (1) Serial in, Parallel

(3) Parallel in Serial

(4) Parallel in, Paral

The shift register car tation of various types of

(1) Serial in serial out

Here n-bit indicate, outed in serial order.

(2) Serial in-Parallel

(3) Parallel- in, Ser

(4) Parallel in, par