Here

CLK	D	Q
0	×	No change
1	0	0
1	1	1

Case 1 : D – High $Q_n = 1$ in fig 4.45

If $D = 1$

Means $S = 1$ & $R = 0$

That's case of S-R Flip-Flop, Flip-Flop is said to be in set state and logic 1 is stored.

Case 2 : D – Low $Q_n = 1$ in fig. 4.45

If $D = 0$

Means $S = 0$ & $R = 1$

That's again case of S-R Flip-Flop, Flip-Flop is said to be in Reset state and logic 0 is stored.

DO YOU KNOW ?

D Flip-Flop is also known as Delay Flip-Flop.

Concluding Case 1 and Case 2

"The output Q follows input D at rising edge of clock pulse".

Truth Table :

Positive edge Triggered clock	D	Q_{n+1}	$\overline{Q_{n+1}}$
↑	1	1	0
↑	0	0	1

4.11 EDGE-TRIGGERED J-K FLIP-FLOP

J-K Flip-Flop is also identical to S-R Flip-Flop but having the advantages that, it does not have invalid state.

Features —

— It's a versatile Flip-Flop

— It avoids the invalid-state condition of S-R Flip-Flop

— It is most widely used Flip-Flop among all Flip-Flops.

— It is most widely used in digital system.

J-K Flip-Flop is derived from S-R Flip-Flop by connecting Q output back with input of N_2 and simultaneously $\overline{Q}$ output back with input of N_1.

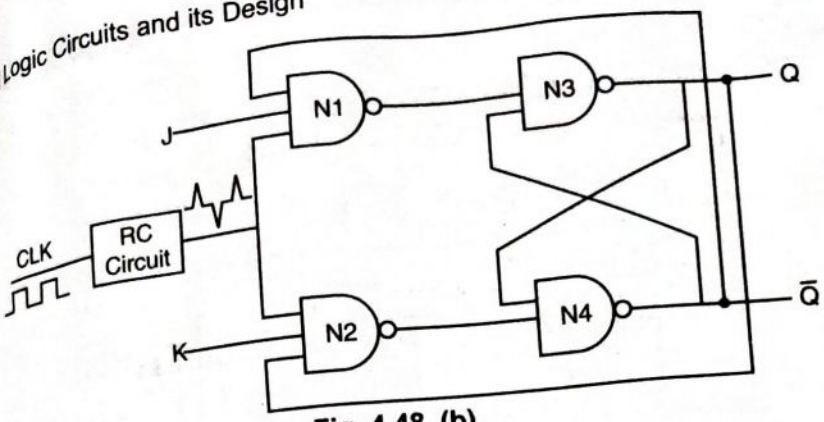


Fig. 4.48. (b)

Case 1 :

$J = 0$

$K = 0$

CLK – High ( ) is shown as Clk = 1

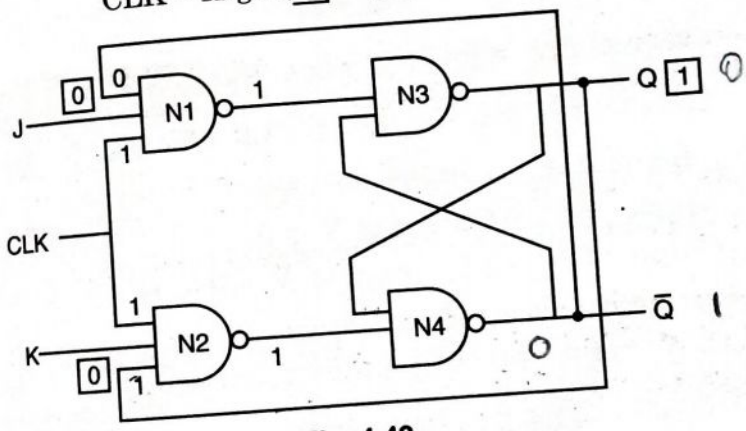


Fig. 4.49.

Let's take $\left.\begin{array}{l} Q = 1 \\ J = 0 \\ K = 0 \end{array}\right]$ Assumption

Output of $N_1 = 1$ ($\because J = 0$, CLK – High = 1, $\bar{Q} = 0$)

Output of $N_2 = 1$ ($\because K = 0$, CLK = 1, $Q = 1$)

$\left.\begin{array}{l} \text{Input of } N_4 = 1 \text{ \& } 1 \\ \text{Hence output of } N_4 = 0 \\ \text{Means } \bar{Q} = 0 \end{array}\right]$ $\because Q$ is coupled back to Input of N_4

$\left.\begin{array}{l} \text{Input of } N_3 = 1 \text{ \& } 0 \\ \text{Hence output of } N_3 = 1 \\ \text{Means } Q = 1 \end{array}\right]$ $\because \bar{Q}$ is coupled back to Input of N_3

Hence there is no change in the output. It is same as that we have initially assumed.

Case 2 :

$J = 0$
$K = 1$ & $Q = 1$
CLK – High ( )

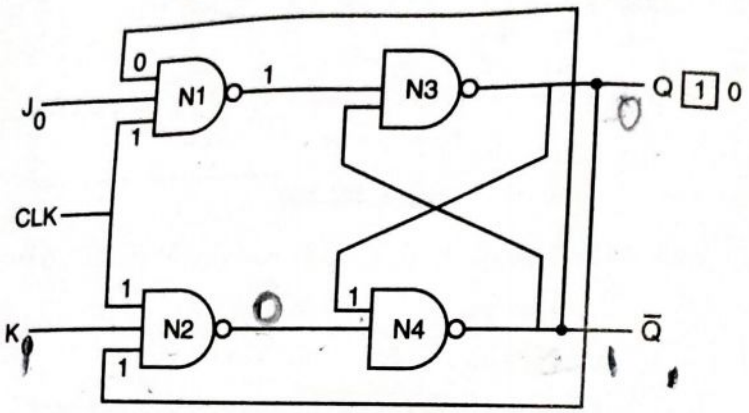


Fig. 4.50.

Output of $N_1 = 1$ ($\because J = 0$, CLK – High ( ), $\overline{Q} = 0$)

Output of $N_2 = 0$ ($\because K = 1$, CLK – High ( ), $Q = 1$)

Input of N_3 = Output of $N_1 = 1$

Input of N_4 = Output of $N_2 = 0$

Output of $N_4 = 1$ [$\because$ Input of $N_4 = 0$ & 1]

Because Q is coupled back to Input of N_4

Output of $N_3 = 0$ [$\because$ Input of $N_3 = 1$ & 0]

Because $\overline{Q}$ is coupled back to Input of N_3

Hence Flip-Flop is said to be reset because $Q = 0$. Previously we have assumed $Q = 1$.

Case 3 :

$J = 1$
$K = 0$ & $Q = 1$
CLK – High ( )

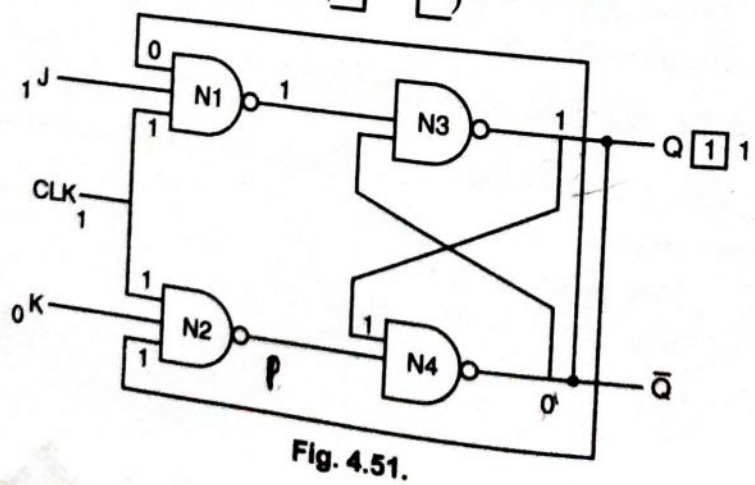


Fig. 4.51.

Output of $N_1 = 1$ ($\because J = 1$, CLK – High ( ), $\overline{Q} = 0$)

Output of $N_2 = 1$ ($\because K = 0$, CLK – High ( ), $Q = 1$)

Input of N_3 = Output of $N_1 = 1$

Input of N_4 = Output of $N_2 = 1$

Output of $N_4 = 0$ [$\because$ Input of $N_4 = 1$ & 1]

$\because Q$ is coupled back to Input of N_4

Output of $N_3 = 1$ [$\because$ Input of $N_3 = 1$ & 0]

$\because \overline{Q}$ is coupled back to Input of N_3

Hence Flip-Flop is said to be set $\because Q = 1$.

Case 4 :

Subcase 1 :

$J = 1$

$K = 1$ & $Q = 1$

CLK – High ( )

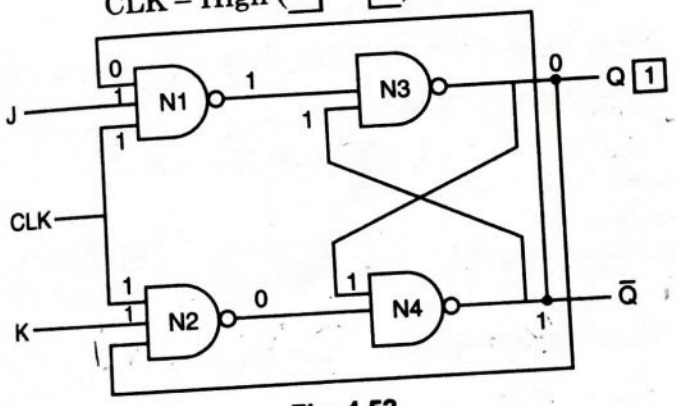


Fig. 4.52.

Output of $N_1 = 1$ ($\because J = 1$, CLK – High ( ), $\overline{Q} = 0$)

Output of $N_2 = 0$ ($\because K = 1$, CLK – High ( ), $Q = 1$)

Input of N_3 = Output of $N_1 = 1$

Input of N_4 = Output of $N_2 = 0$

Output of $N_4 = 1$ [$\because$ Input of $N_4 = 0$ & 1]

Because Q is coupled back to Input of N_4

Output of $N_3 = 0$ [$\because$ Input of $N_3 = 1$ & 1]

Because $\overline{Q}$ is coupled back to Input of N_3

Subcase 2 :

$J = 1$

$K = 1$ & $Q = 0$

CLK – High ( )

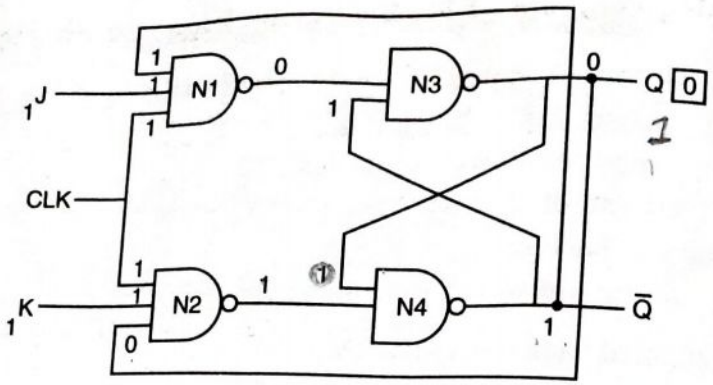


Fig. 4.53.

Output of $N_1 = 0$ ($\because J = 1$, CLK – High ( ), $\bar{Q} = 1$)

Output of $N_2 = 1$ ($\because K = 1$, CLK – High ( ), $Q = 0$)

Input of N_3 = Output of $N_1 = 0$

Input of N_4 = Output of $N_2 = 1$

Output of $N_3 = 1$ [$\because$ Input of $N_3 = 0$ & 1]

$\because \bar{Q}$ is coupled back to Input of N_3

Output of $N_4 = 0$ [$\because$ Input of $N_4 = 1$ & 1]

$\because Q$ is coupled back to Input of N_4

We conclude from subcase 1 and subcase 2 that, Flip-Flop revert its state. It goes to opposite state. This condition is most commonly known as Toggle condition.

Hence Flip-Flop is said to be set $\because Q = 1$.

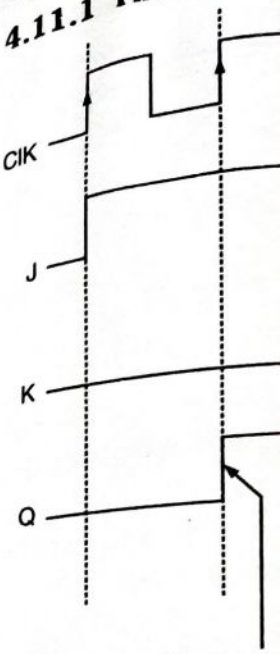
Truth Table

Q_0 – Previous output

CLK	J	K	Q	$\bar{Q}$
⎍	0	0	Q_0	$\bar{Q}_0$ (No change)
⎍	0	1	0	1 (Set)
⎍	1	0	1	0 (Reset)
⎍	1	1	$\bar{Q}_0$	Q_0 (Toggle)

Note: If we had level triggering instead of edge triggering, then if CLK = 1, $J = 1$, $K = 1$. This causes output to get complemented again and again until CLK becomes zero. This condition is undesired and hence to avoid this condition, we have taken clock pulse with edge triggering.

4.11.1 Timing Di



Flip flop is
Q = 1 at J =
CLK = ↑ (

Here

CLK
0
1
↓
×
↑
↑
↑

4.12 PRESET AND

They are used to se
input i.e., in order
known as preset (P

These inputs a
synchronism with t
The signals S-R, J-
these inputs are tra
of the clock pulse
pulse. A D type flip

4.11.1 Timing Diagram of Positive Edge Triggered JK Flip Flop

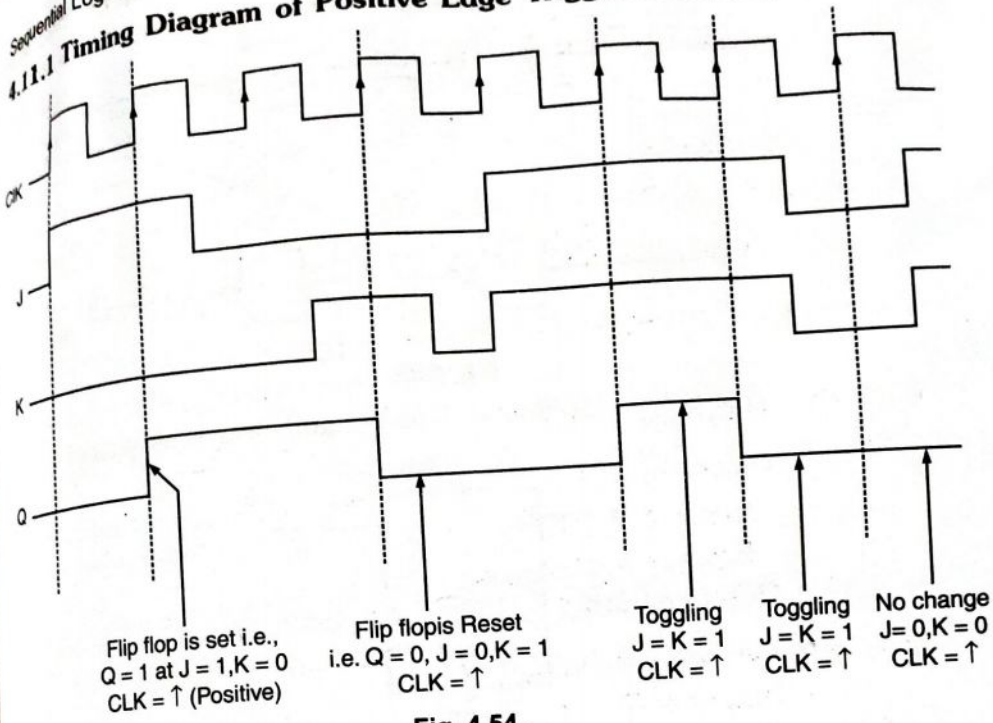


Fig. 4.54.

Here

CLK	J	K	Q
0	×	×	No change (NC)
1	×	×	No change (NC)
↓	×	×	No change (NC)
×	0	0	No change (NC)
↑	0	1	0 (Reset)
↑	1	0	1 (Set)
↑	1	1	Toggle

4.12 PRESET AND CLEAR SIGNAL

They are used to set or reset the state of flip flop regardless of the state of clock input i.e., in order to assign the initial state of the flip flop. These inputs are known as preset (Pr) or direct set (S_D) and clear (Cr) or direct reset (R_D)

These inputs are applied at any time between clock pulses and is not synchronism with the clock pulse. It means that they are asynchronous signals. The signals S-R, J-K and D are synchronous signal or inputs because data on these inputs are transferred to the flip flops output only on the triggering edge of the clock pulse means data are transferred synchronously with the clock pulse. A D type flip flop with preset and clear signal is shown as follows :

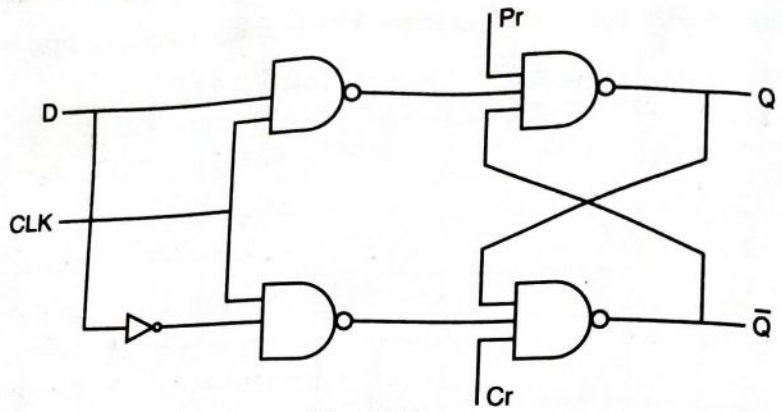


Fig. 4.55.

Logic symbol of *D* type flip flop with preset and clear is shown below :

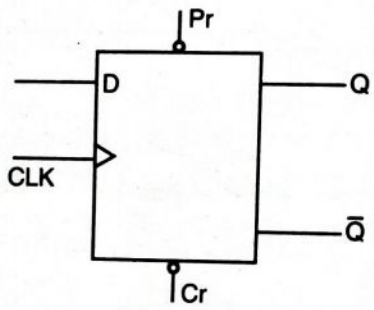


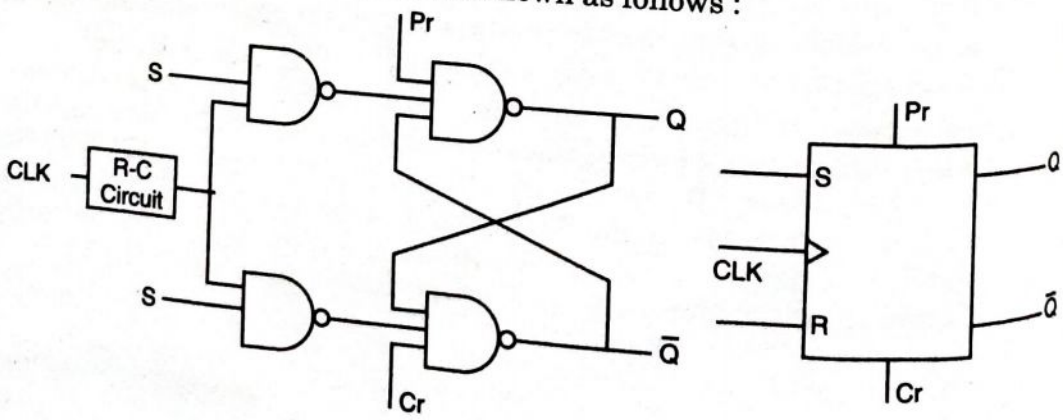
Fig. 4.56.

They are generally active low signal. The truth table is shown as follows:

	Inputs		Output	Operation
CLK	*Cr*	*Pr*	*Q*	Performed
1	1	1	Q_{n+1}	Normal flip flop
0	1	0	1	Preset (Set)
0	0	1	0	Clear (Reset)
0	0	0	—	Uncertain

For Clocked S-R Flip Flop

The preset and clear inputs are shown as follows :



(a) Circuit diagram (a) Logic symbol

Fig. 4.57.

Here
When Clk = 1, $S = 1$ & $R = 0$, then output = 1 and
When Clk = 1, $S = 0$ & $R = 1$, then output = 0
and in that case, the $Pr = Cr = 1$, works as clocked S-R flip flop (normal flip flop).

The $Pr = Cr = 1$, takes the low value because inside the circuit $\overline{Pr}$ and $\overline{Cr}$ are present and high on both the inputs make them low and hence, the circuit works as normal clocked S-R flip flop.

When Clk = 0, $Cr = 0$ & $P_r = 1$, then clear operation is performed by the circuit because $Cr(\overline{Cr})$ is activated as they are active low signal means worked, when it is low i.e., '0'.

When Clk = 0, $Cr = 1$ & $Pr = 0$, then preset means set operation is performed by the circuit.

The truth table is given as follows :

Inputs			Outputs	Operation Performed
CLK	Cr	Pr	Q_n	
1	1	1	Q_{n+1} (Clocked S-R operation)	Normal flip flop
0	0	1	0 (Reset)	Clear
0	1	0	1 (set)	Preset

Application Area

They are used when multiple flip flops are ganged together to perform a function on a multi-bit binary word and a single line is needed to set or reset them all at once.

Summary

- Preset and clear are asynchronous signals or inputs.
- Both are active low signal.
- When $Pr = 0$ and $Cr = 1$, then Preset operation is performed in the circuit.
- When $Pr = 1$ and $Cr = 0$, then clear operation is performed in the circuit.
- When $Pr = Cr = 1$, then circuit perform normal flip flop operation.

4.13 T FLIP-FLOP (TRIGGER / TOGGLE FLIP-FLOP)

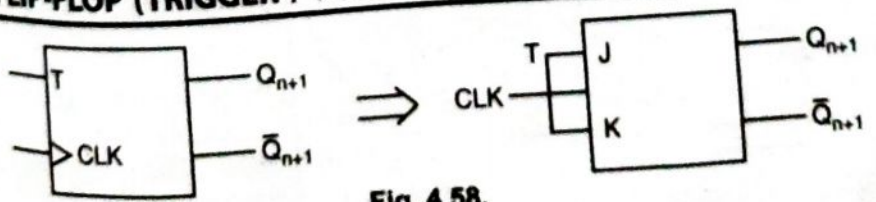


Fig. 4.58.

If we connect J & K inputs together in a J-K Flip-Flop, then we can label common connection of J-K Flip-Flop as T input.

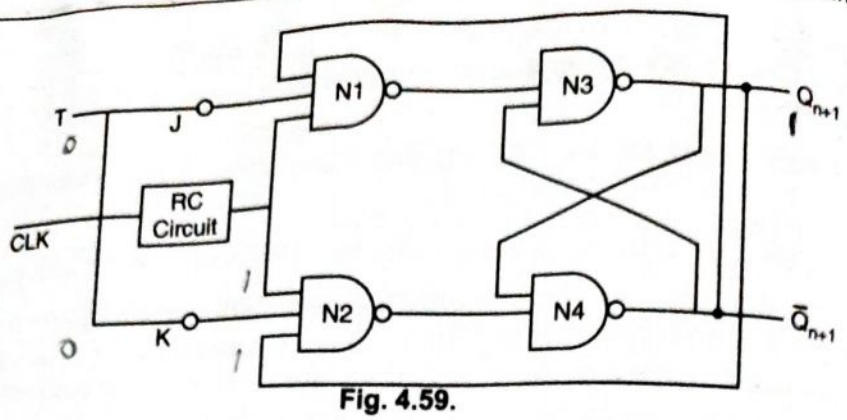


Fig. 4.59.

Case 1 : $T = 0$ Means $J = 0 \quad K = 0$ $Q_n = 1$

Then there is no change in the output (as seen in edge-triggered J-K Flip-Flop) $Q_{n+1} = 1$

Case 2 : $T = 1$ Means $J = 1 \quad K = 1$ $Q_n = 1$

Then there is reverse of state of output (as compare to previous Input)

Hence $Q_{n+1} = 0$

Concluding Remarks

If $T = 1$ and $Q_n = 0$ (Previous), Then $Q_{n+1} = 1$ (Present)

Otherwise

If $T = 1$ and $Q_n = 1$ (Previous), Then $Q_{n+1} = 0$ (Present)

Means output will change its state from 0 to 1 or 1 to 0. This process is called toggling. That's why T Flip-Flop is also called as Toggle Flip-Flop.

Hence

T	Q_n (Previous)	Q_{n+1} (Present)	
0	0	0	No change in previous output
0	1	0	
1	0	1	Complemented output of previous output
1	1	0	

i.e., Truth table of T flip flop

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

DO YOU KNOW ?

T Flip Flops are most commonly used in binary counters, because of its divide-by-2 capability.

4.14 RACE AROUND CONDITION

In case of level triggered JK flip flop when $J = K = 1$, then output $Q_{n+1} = \overline{Q_n}$ i.e., output is the invert of previous output and this yields to continuous change

in value of Q_{n+1} from zero to one and one to zero in a single clock pulse is term as race around condition.

A condition in which $J = K = 1$ and the output is continuously changes from 0 to 1 and 1 to 0 in a single clock pulse is called race around condition.

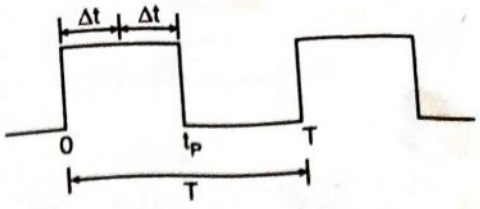


Fig. 4.60. (a)

If Δt is the propagation delay of flip flop i.e., after Δt time, flip flop changes its output and T is total time of one clock pulse then for race around condition this equation must satisfied :

$$0 < \Delta t < t_p \quad \text{— Equation}$$

Where t_p is time period where pulse is high.

Methods to Remove Race-Around Condition

There are three methods to remove race-around condition which are as follows :

(1) Use Edge-Triggered flip flop.

(2) Flip flop must follows the following equation

$$t_p < \Delta t < T$$

means Δt (Propagation delay) must be greater than t_p (time period when pulse is high) and lesser than T (total time period of pulse). In above condition flip flop calculate its value one time in one clock pulse.

(3) Use of Master-slave flip flop to lock the output for complete clock cycle.

4.15 MASTER SLAVE J-K FLIP-FLOP

It's a cascade of two flip-flops in which first one responds to data inputs when clock is high whereas second one responds to output of first one when clock is low.

Hence final output changs only when clock is low, when data inputs are not effective. Hence race around condition gets eliminated.

In this way first flip-flop is known as master and second flip-flop is known as slave.

Master F/F	+	Slave F/F	⇒	Master-slave F/F
⇓		⇓		
Positively clocked		Negatively clocked		

When CLk is High: Master will be active and slave will be deactive (because Inverted CLK of master is provided to slave)

When CLK is Low : Master will be deactive and slave will be active

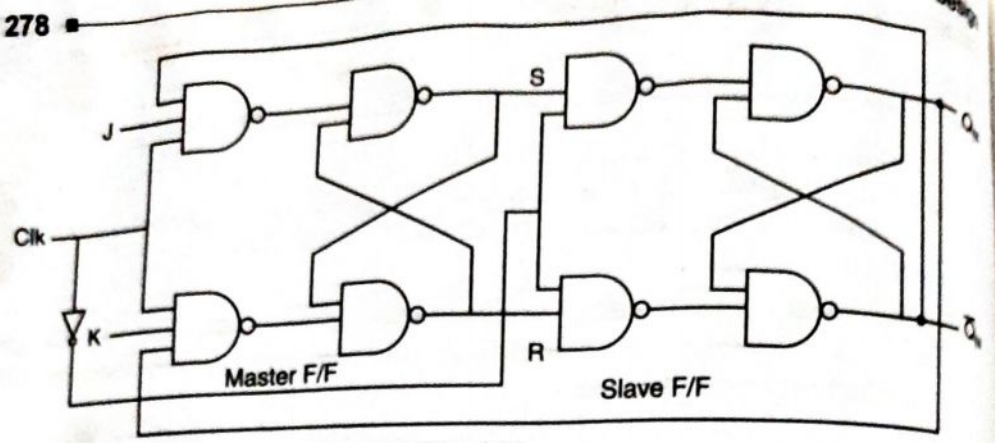


Fig. 4.61.

Let's assume that Q_N and $\bar{Q}_N$ are present outputs of S-R flip-flop i.e, slave flip-flop and most precisely of master-slave flip-flop.

Similarly Q_{N+1} and $\overline{Q_{N+1}}$ are next state outputs of S-R flip-flop i.e., slave flip-flop and most precisely of Master-slave Flip-flop.

We also assume that Q_1 and $\bar{Q}_1$ are present state outputs of J-K flip-flop i.e, Master flip-flop.

Similarly Q_2 and $\bar{Q}_2$ are next state outputs of J-K flip-flop i.e., master flip-flop.

Now it is very important to observe that Q_2 and $\bar{Q}_2$ are driving S and R inputs of slave flip-flop respectively.

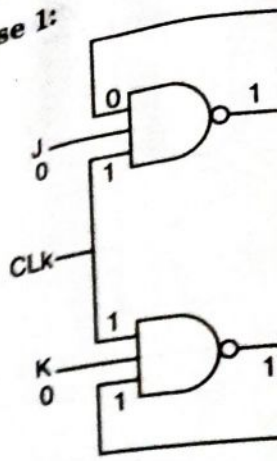
It means $S = Q_2$

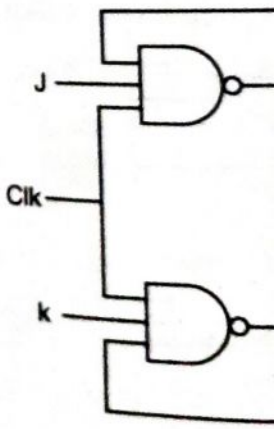
$$R = \bar{Q}_2$$

It is also necessary to observe that if we assume $Q_N = 0$ and $\bar{Q}_N = 1$, then we have to automatically assume $Q_1 = 0$ and $\bar{Q}_1 = 1$. Because it is not possible to achieve $Q_N = 0$ and $\bar{Q}_N = 1$ if $S = Q_1 = 1$ and $R = \bar{Q}_1 = 0$.

Similarly if we assume $Q_N = 1$ and $\bar{Q}_N = 0$. Then we have to automatically assume Q1 = 1 and $\bar{Q}_1 = 0$ because it is not possible to achieve $Q_N = 1$ and $\bar{Q}_N = 0$ if $S = Q_1 = 0$ and $R = \bar{Q}_1 = 1$.

Case 1:





Note: The valu

Case I:

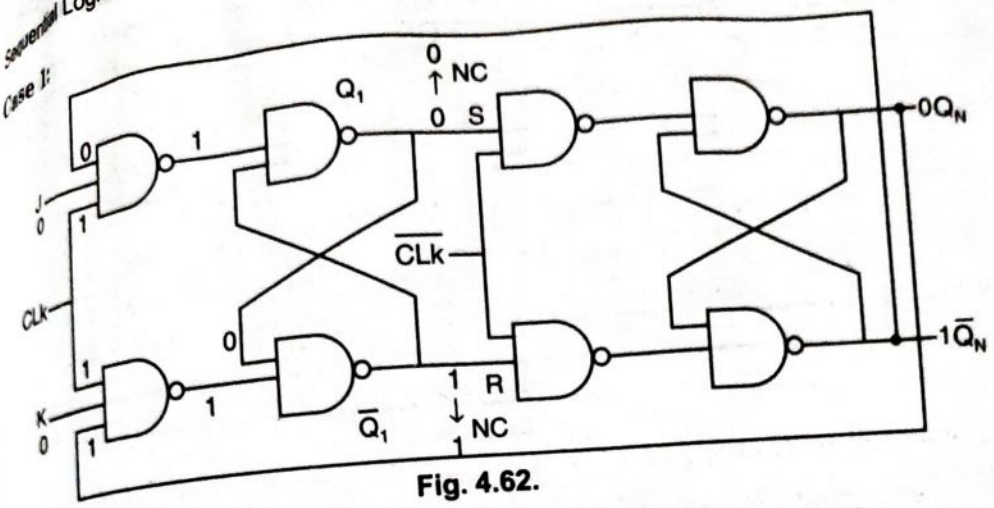


Fig. 4.62.

Master	J	K	Q_N	$\bar{Q}_N$
Active	0	0	0	1

Q_1	$\bar{Q}_1$	Q2	$\bar{Q}_2$
0	1	0	1

Assumed present state of J-K F/F

Obtained Next states of J-K F/F

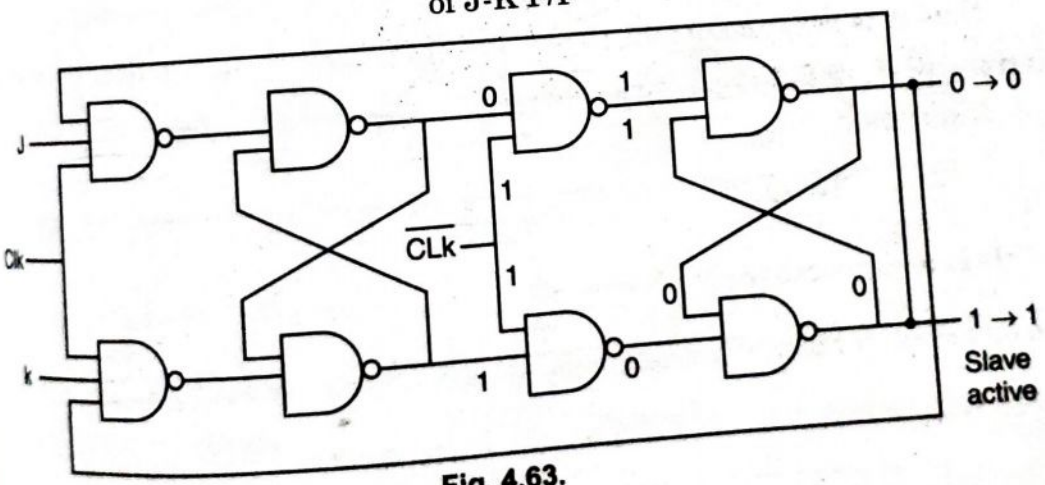


Fig. 4.63.

Q_N	$\bar{Q}_N$
0	1

Assumed present state of S-R F/F

Q_{N+1}	$\bar{Q}_{N+1}$
0	1

Obtained next state of S-R F/F

Note: The values of Q_1 and $\bar{Q}_1$ must be same with Q_N and $\bar{Q}_N$

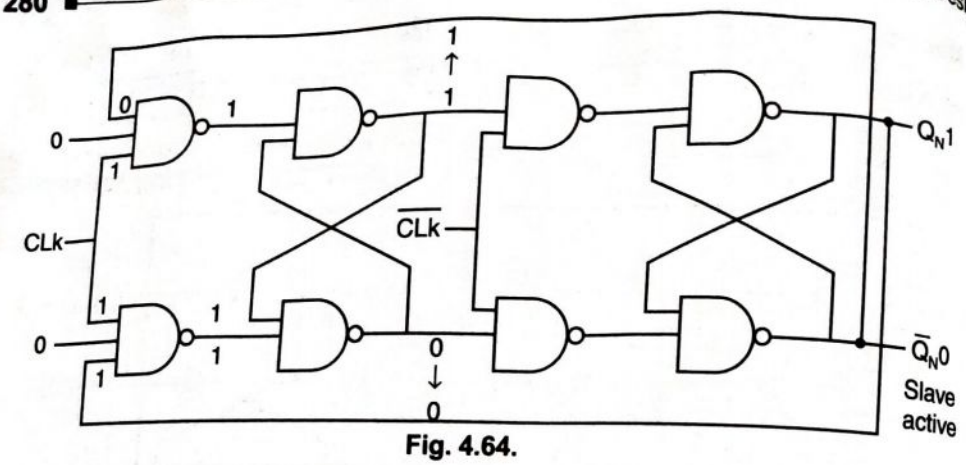


Fig. 4.64.

Master	J	K	Q_N	$\bar{Q}_N$	Q_1	$\bar{Q}_1$	Q_{N+1}	$\bar{Q}_{N+1}$
Active	0	1	1	0	1	0	1	0

Assumed present stae of J-K F/F

Obtained next state of J-K F/F

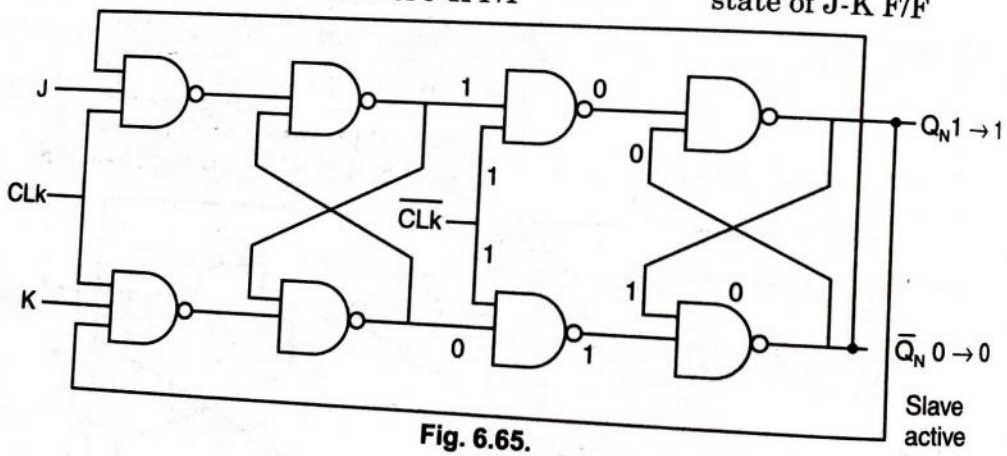


Fig. 6.65.

Q_N	$\bar{Q}_N$
1	0

Assumed present state of S-R F/F

Q_{N+1}	$\bar{Q}_{N+1}$
1	0

Obtained next state of S-R F/F

Case 2

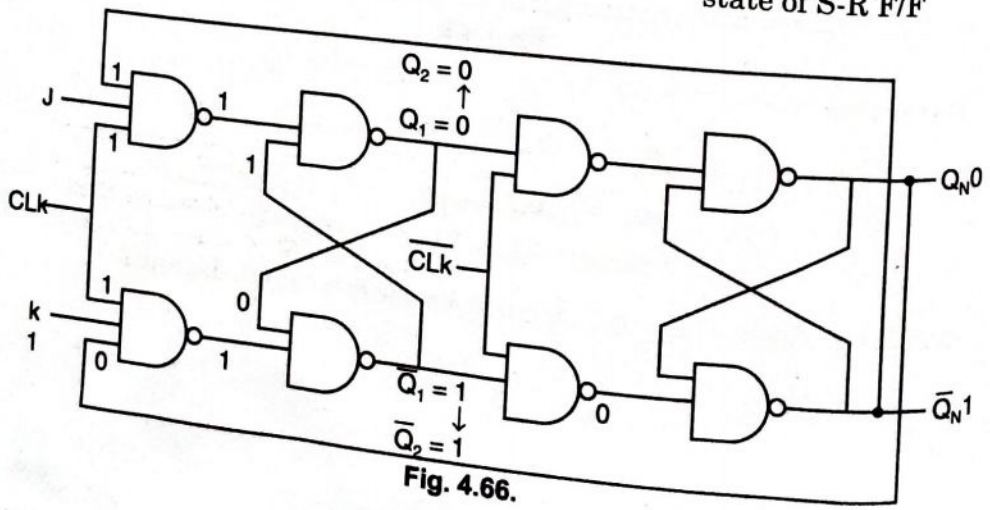
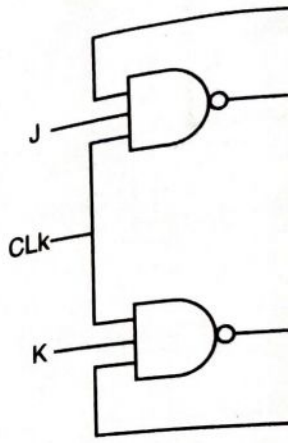


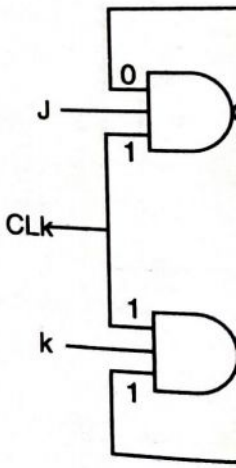
Fig. 4.66.

Master active

J	K
0	1



Slave active



Master active

	J	K	Q_N	$\bar{Q}_N$	Q_1	$\bar{Q}_1$	Q_{N+1}	$\bar{Q}_{N+1}$
Master active	0	1	0	1	0	1	0	1

Assumed present stae of J-K F/F — Obtained next state of J-K F/F

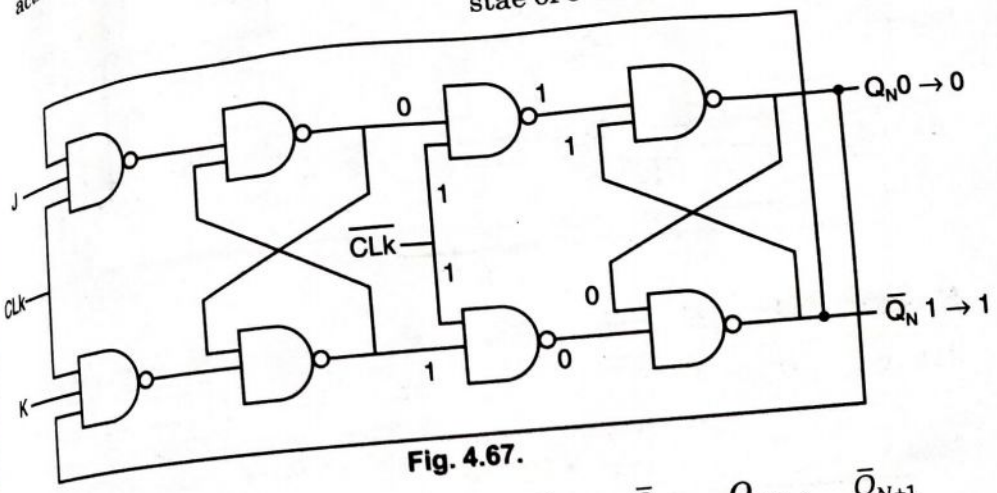


Fig. 4.67.

	J	K	Q_N	$\bar{Q}_N$	Q_{N+1}	$\bar{Q}_{N+1}$
Slave active	0	1	0	1	0	1

Assumed present stae of S-R F/F — Obtained next state of S-R F/F

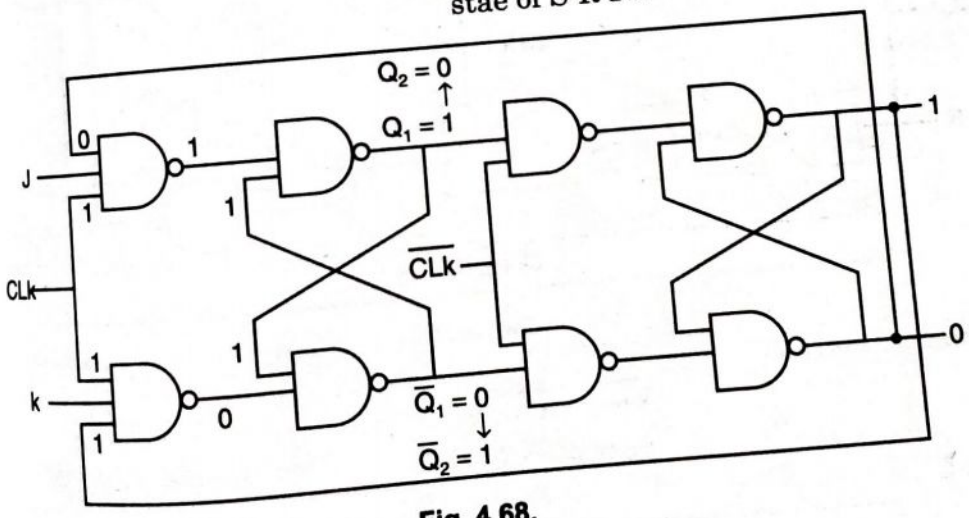


Fig. 4.68.

Master active

J	K	Q_N	$\bar{Q}_N$	Q_1	$\bar{Q}_1$	Q_2	$\bar{Q}_2$
0	1	1	0	1	0	0	1

Assumed present state of J-K F/F master F/F — Obtained Next state of J-K F/F Master F/F

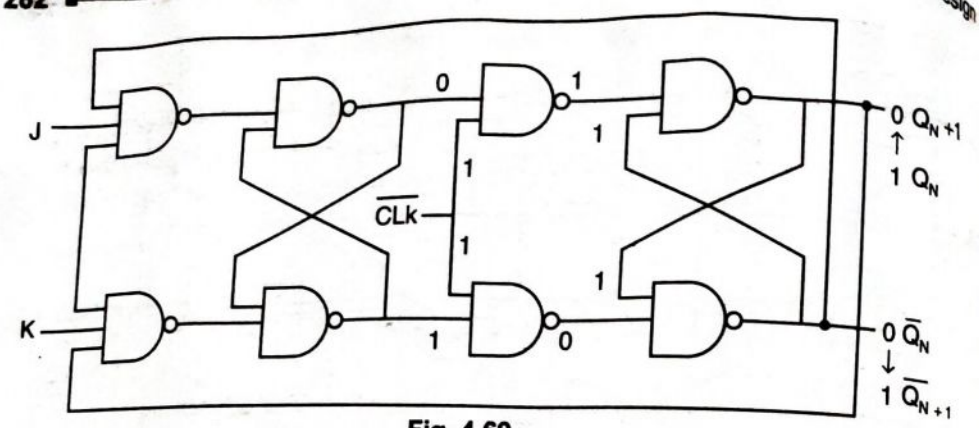


Fig. 4.69.

Slave Active	J	K	Q_N	$\bar{Q}_N$	Q_{N+1}	$\bar{Q}_{N+1}$
	0	1	1	0	0	1

Assumed present state of S-R F/F — Obtained Next state of S-R F/F

Case 3

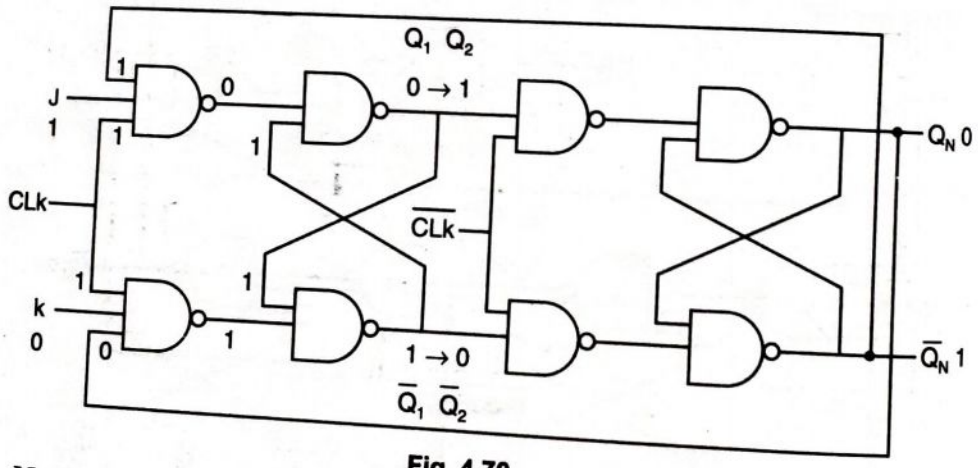
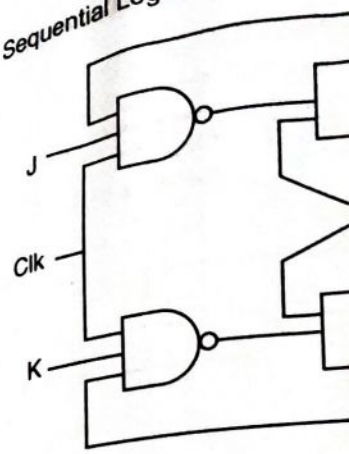


Fig. 4.70.

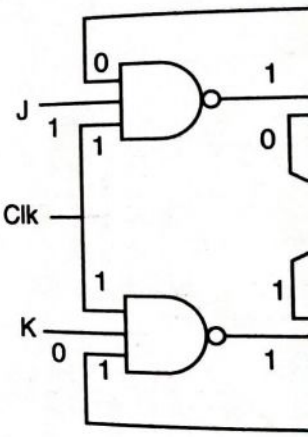
Master active

J	K	Q_N	$\bar{Q}_N$	Q_1	$\bar{Q}_1$	Q_2	$\bar{Q}_2$
1	0	0	1	0	1	1	0

Assumed present J-K F/F — Obtained Next state of J-K F/F

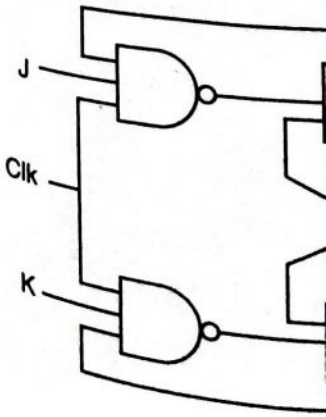


Slave active



Master active J K

1 0



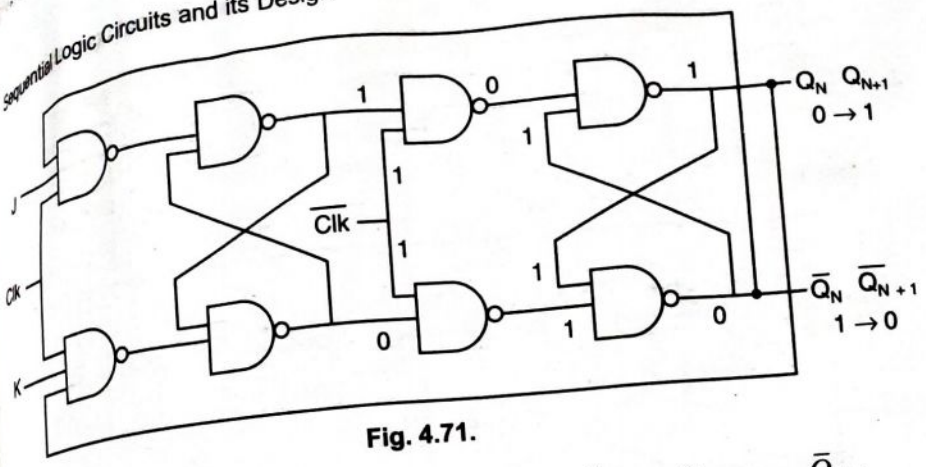


Fig. 4.71.

Slave active

Q_N	$\overline{Q}_N$
0	1

Assumed present S-R F/F

Q_{N+1}	$\overline{Q}_{N+1}$
1	0

Obtained Next state of S-R F/F

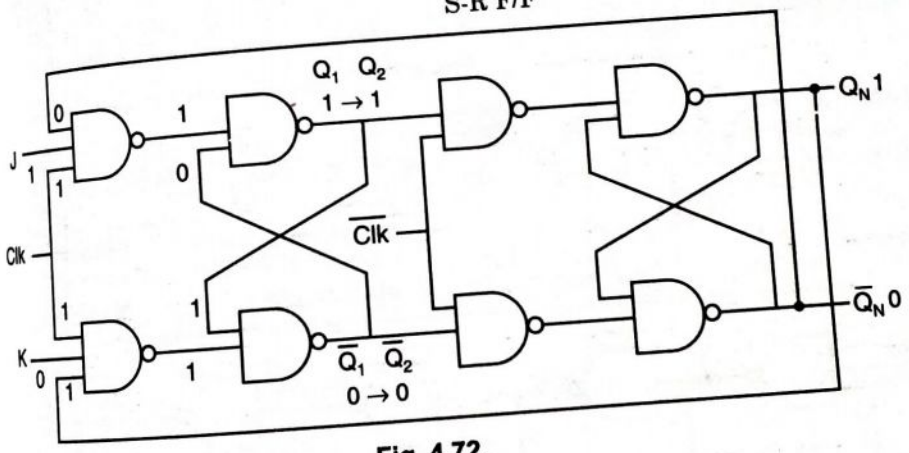


Fig. 4.72.

Master active J K Q_N $\overline{Q}_N$

1 0 1 0

Q_1	$\overline{Q}_1$
1	0

⇓

Assumed present state J-K F/F

Q_2	$\overline{Q}_2$
1	0

⇓

Obtained Next state of J-K F/F

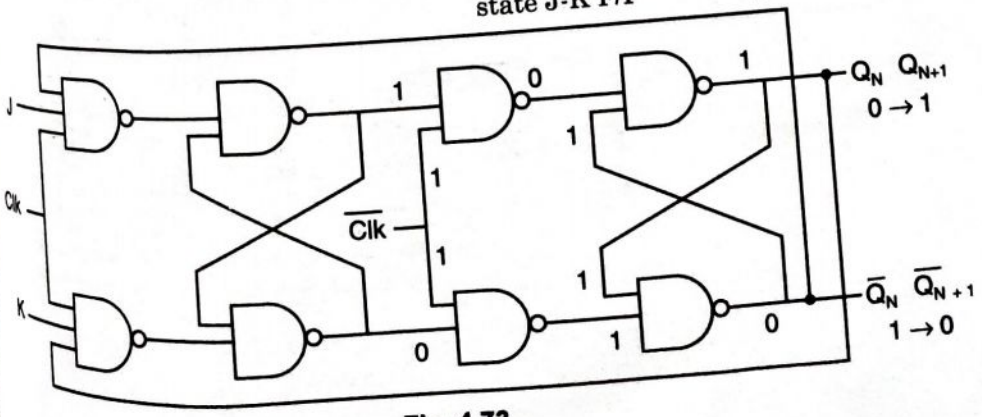


Fig. 4.73.

	J	K	Q_N	$\bar{Q}_N$	Q_{N+1}	$\bar{Q}_{N+1}$
Slave Active	1	0	0	1	1	0

Assumed present state of S-R F/F

Obtained Next state of S-R F/F

Case 4

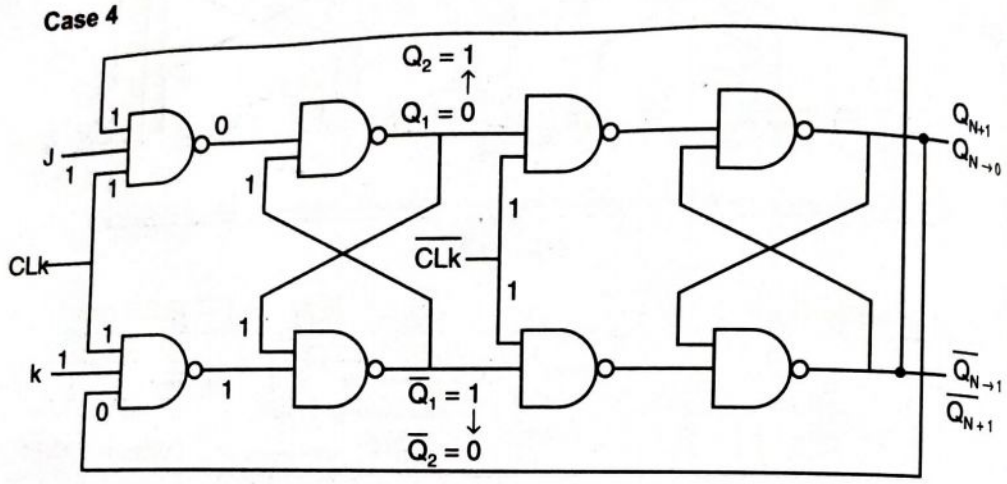


Fig. 4.74.

Master	J	K	Q_N	$\bar{Q}_N$	Q_1	$\bar{Q}_1$	Q_2	$\bar{Q}_2$
Active	1	1	0	1	0	1	1	0

Assumed present state of J-K F/F/ Master F/F

Obtained Next state of J-K F/F/ Master F/F

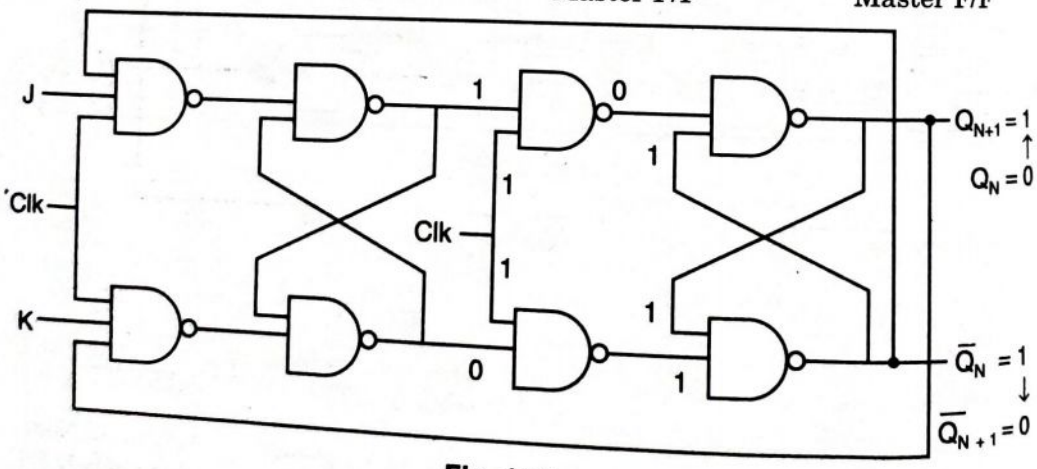


Fig. 4.75.

Slave active	J	K	Q_N	$\bar{Q}_N$	Q_{N+1}	$\bar{Q}_{N+1}$
	1	1	0	1	1	0

Assumed present state of S-R F/F

Obtained Next state of S-R F/F

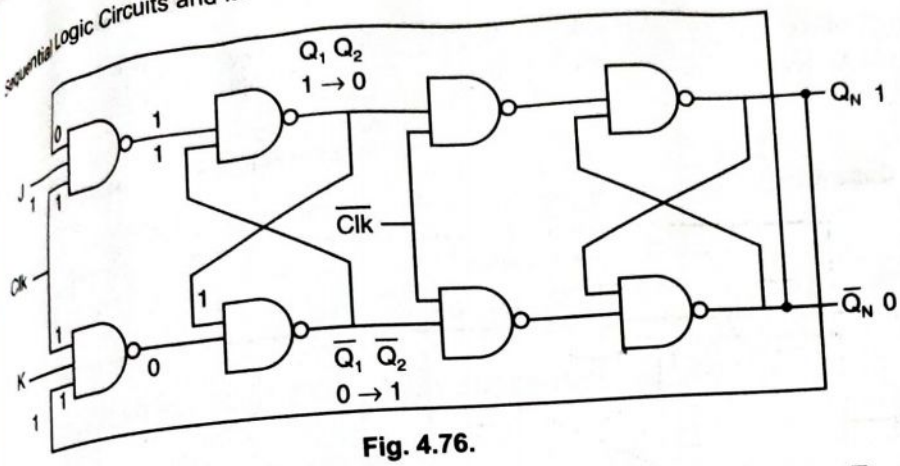


Fig. 4.76.

	J	K	Q_N	$\overline{Q}_N$	Q_1	$\overline{Q}_1$	Q_2	$\overline{Q}_2$
Master active	1	1	1	0	1	0	0	1
					⇓ Assumed present state of J-K F/F F/F		⇓ Obtained Next state of J-K F/F	

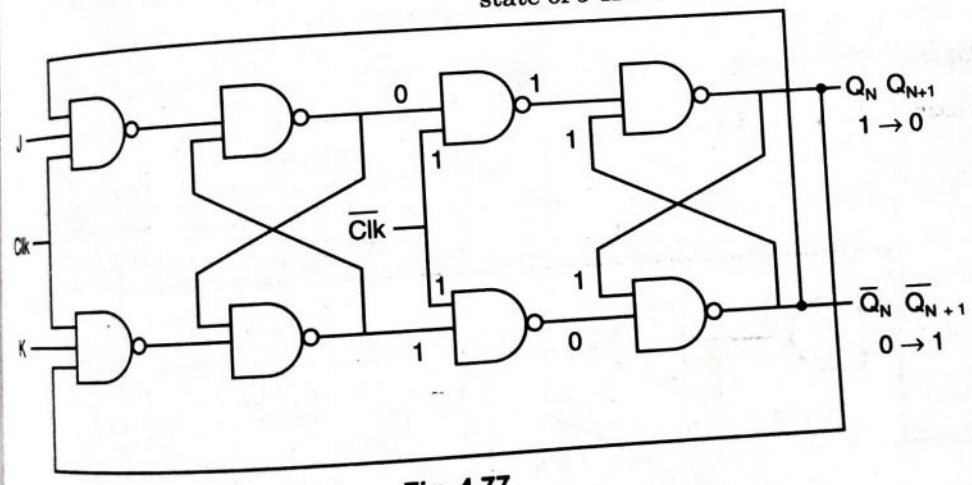


Fig. 4.77.

	J	K	Q_N	$\overline{Q}_N$	Q_{N+1}	$\overline{Q}_{N+1}$
Slave active	1	1	1	0	0	1
			⇓ Assumed present state of S-R F/F		⇓ Obtained Next state of S-R F/F	

Truth table (Characteristic table of master slave J-K flip flop)

	J	K	Q_1	$\overline{Q}_1$	Q_2	$\overline{Q}_2$	S	R	Q_N	$\overline{Q}_N$	Q_{N+1}	$\overline{Q}_{N+1}$
CLk = 1	0	0	0	1	0	1			0	1	Slave dective	
CLk = 0	Master -Deactive						0	1	0	1	0	1
CLk = 1	0	0	1	0	1	0	No change		1	0	Slave deactive	
CLk = 0	Master - Deactive						1	0	1	0	1	0
	No change condition of master during + Ve Clk pulse is copied by slave during – Ve											
CLk = 1	0	1	0	1	0	1			0	1	Slave decative	
CLk = 0	Master - Deactive						0	1	0	1	0	1
CLk = 1	0	1	1	0	0	1	Reset		1	0	Slave decative	
CLk = 0	Master - Deactive						0	0	1	0	0	1
	This process shown in case 2 is known as cocking. Reset of master during +ve clk is copied by slave during – ve Clk											
CLk = 1	1	0	0	1	1	0			0	1	Slave deactive	
CLk = 0	Master - Deactive						1	0	0	1	1	0
CLk = 1	1	0	1	0	1	0	Set		1	0	Slave deactive	
CLk = 0	Master - Deactive						1	0	1	0	1	0
	This process shown in case 3 is also cocking. Set state of master during + Ve Clk is copied by slave during – Ve Clk											
CLk = 1	1	1	0	1	1	0			0	1	Slave deactive	
CLk = 0	Master - Deactive						1	0	0	1	1	0
CLk = 1	1	1	1	0	0	1	Toggle		1	0	Slave deactive	
CLk = 0	Master-Deactive						0	1	1	0	0	1
	Clocking process is continued here also											
	Toggling of master during + Ve CLk pulse is copied by slave during – Ve CLk pulse											

Action done by master during +Ve CLK is just copied by slave during – VE CLK.

⇓ This process is called as

Cocking

How Race around condition gets avoided in Master slave J-K Flip Flop

If

$$J = K = 1$$

CLK = 1 Then master toggles but slave remains deactive.

Similarly

When CLK = 0 Then slave toggles but master remains deactive.