Here

Clk	R	S	Q
Low	×	×	No change
High	0	0	No change
High	0	1	1
High	1	0	0
High	1	1	* (Race)

4.7. FLIP-FLOP

"A basic memory element & a bistable device which remains either in state 1 or state 0". Flip-Flops are again sequential circuits because of feedback arrangement associated with it. Flip-Flops are basically synchronous/clocked sequential logic circuits, for which change in output takes place in synchronization with the clock.

DO YOU KNOW ?

Clock is a square wave signal, used to synchronize overall action of system.

It must be clear from above paragraph that Latches and Flip-Flops are similar but Flip-Flop is modified form of Latch with additional control input (Clock/Enable). In this way, we can better control the output.

Clock is basically used to control Flip-Flops.

FF में clock होता है

Clock can be classified into two categories :

(1) Positive clocking
(2) Negative clocking

(1) Positive Clocking

If Flip-Flop changes its state at high clock pulse, then Flip-Flop is said to have positive clocking (based on applied Input).

(2) Negative Clocking

If Flip-Flop changes its state (based on applied Input), then Flip-Flop is said to have negative clocking.

Let's take an R-C circuit and try to understand, how we can utilize clock for triggering Flip-Flops.

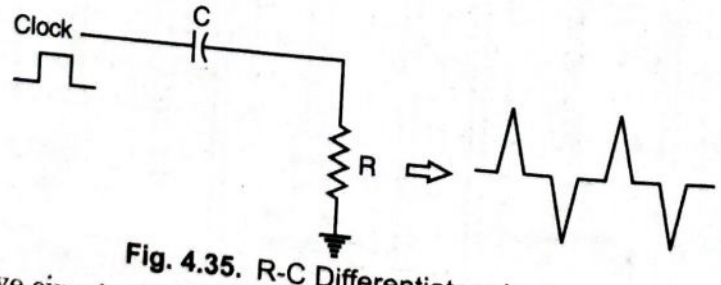


Fig. 4.35. R-C Differentiator circuit.

In the above circuit, value of R and C is taken in such a way that :

$$\tau = RC << t$$

where t is time period of clock pulse.

Let's take High clock pulse and hence capacitor C gets fully charged and rising edge of clock pulse produces positive spike and trailing edge of clock pulse

produces negative spike across resistances R. Clock pulse in the form of spikes is provided to NAND gates. Gates are activated on positive spike and hence Flip-Flop responds according to the applied inputs. This process is most commonly known as edge triggering.

It can be classified into two categories :

(1) Positive edge triggering

(2) Negative edge triggering

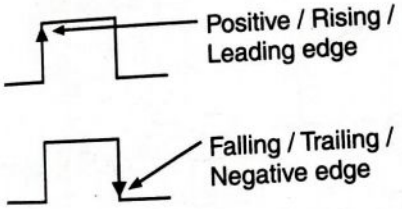
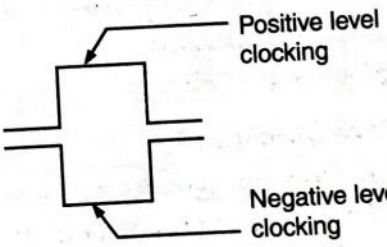
(1) Positive Edge Triggering

If Flip-Flop responds on positive going edge of clock, then Flip-Flop is said to have positive edge triggering.

(2) Negative Edge Triggering

If Flip-Flop responds on negative going edge of clock, then Flip-Flop is said to have negative edge triggering.

Let's make some differences between edge triggering and level triggering.

Edge Triggering	Level Triggering
(1) For edge triggering clock,change in output takes place only on rising edge or falling edge of clock pulse. 	(1) For level triggering clock, change in output takes place on high clock or low clock. 
(2) Output can change only at one instant.	(2) Output can change during entire positive level of clock or entire negative level of clock.
(3) The possibility of undergoing multiple changes in output with respect to any change in input for a particular edge of clock is almost negligible and hence it is having wider scope in master slave flip-flop.	(3) The possibility of undergoing multiple changes in output with respect to any change in input for a particular level of clock is more in level triggering and hence there are more chances of unstability.

4.8 EDGE TRIGGERED S-R FLIP-FLOP

The circuit diagram for edge triggered flip flop is shown as below :

DO YOU KNOW ?

S-R flip flop is basic by which D and JK flip flop can be derived.

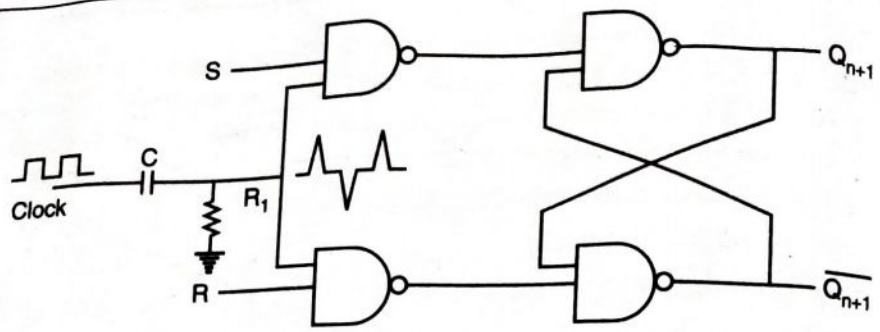


Fig. 4.36.

Here, the clock signal is passed to *R, C* circuit which is known as RC circuit which converts the clock signal into spikes. Let's take different cases to explain functionality of edge triggered *S-R* flip flop.

Case 1 : $S = 0$, $R = 0$ & Clk – Low (is shown as Clk = 0 or ↓) & $Q_n = 0$

This is the case of initialization of flip flop and flip flop is assumed to be reset because $Q_n = 0$.

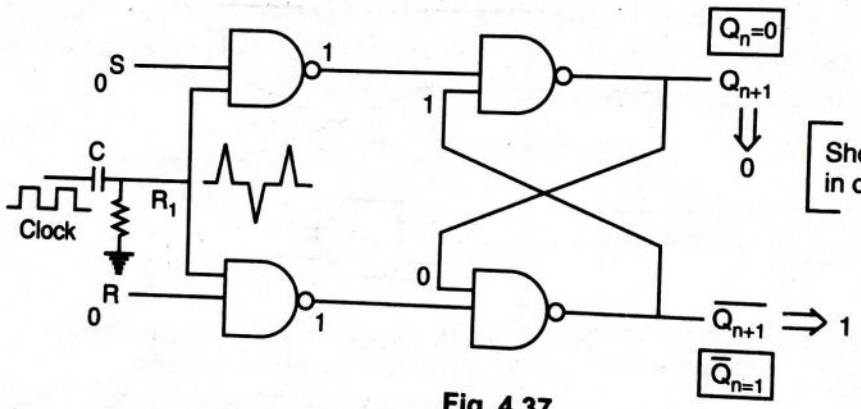


Fig. 4.37.

Now let's make clock pulse high (means clock pulse = 1 or ↑). This time we assume $Q_n = 1$

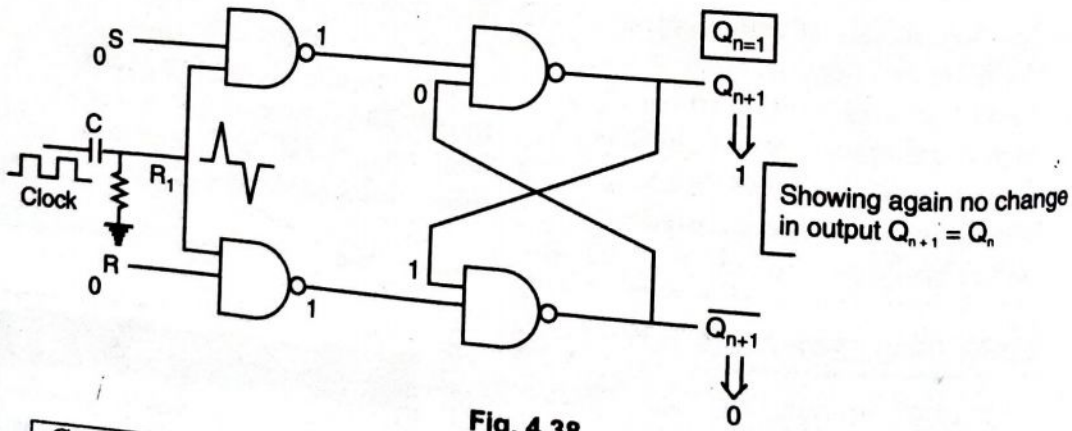


Fig. 4.38.

Case 2 : $S = 1$, $R = 0$ & Clock – High ( ) & $Q_n = 1$

Subcase 1 :

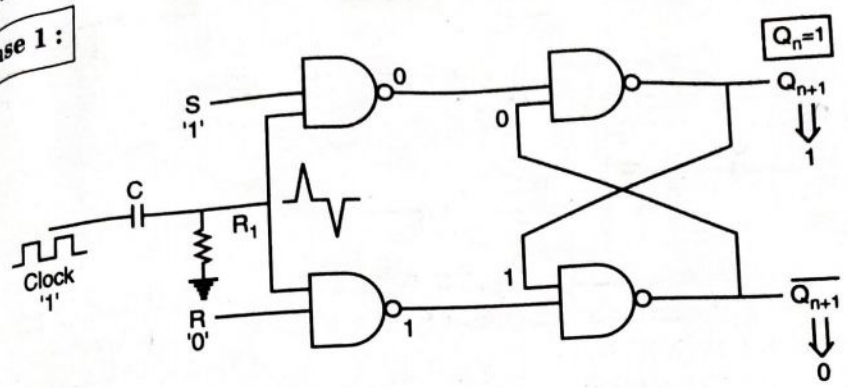


Fig. 4.39. (a)

Let's reverse the situation and take $Q_n = 0$

Subcase 2 :

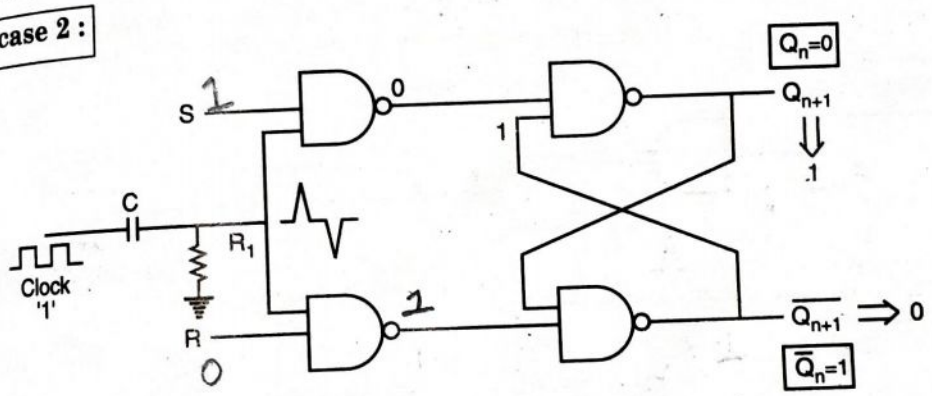


Fig. 4.39. (b)

From case 2 : subcase 1 and subcase 2, we can conclude that, flip-flop is in set state.

Case 3 : $S = 0$, $R = 1$ & Clock = High or ↑ & $Q_n = 1$

Subcase 1 :

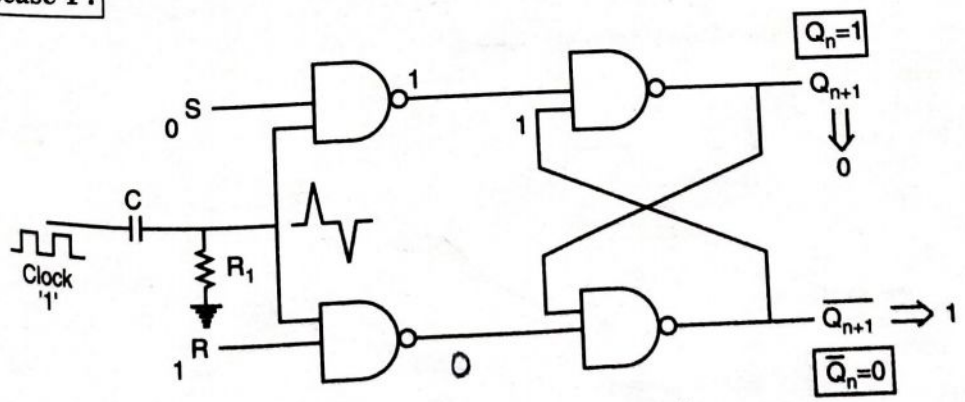


Fig. 4.40.

Let's reverse the situation and take $Q_n = 0$

Subcase 2 :

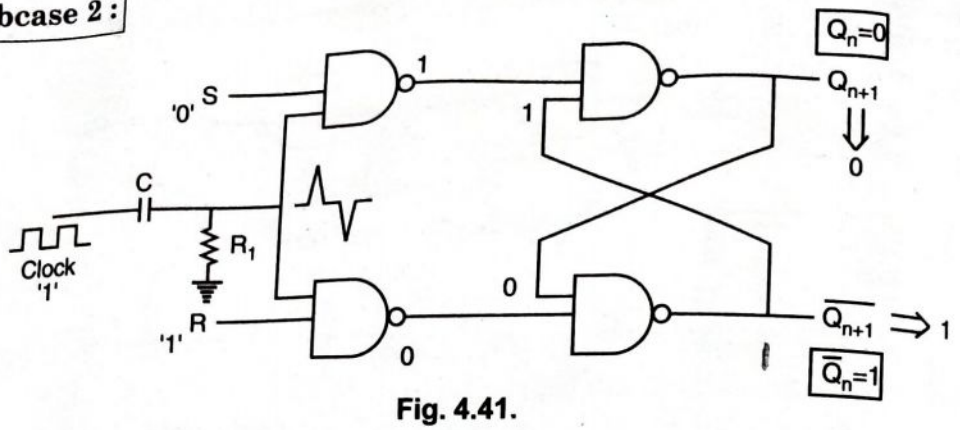


Fig. 4.41.

From case 3 : subcase 1 and subcase 2, we can conclude that, flip-flop is in Reset or Clear state.

Case 4 : $S = 1$, $R = 1$ & Clock = High or ↑ & $Q_n = 1$

Subcase 1 :

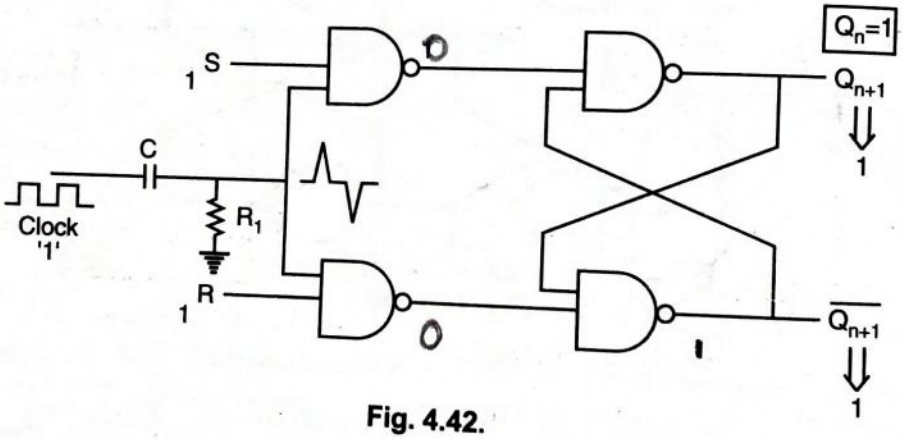


Fig. 4.42.

$Q_{n+1} = \overline{Q_{n+1}} = 1$

[Violating the statement that $\overline{Q_{n+1}}$ is complement of Q_{n+1}]

Let's reverse the situation and take $Q_n = 0$.

Subcase 2 :

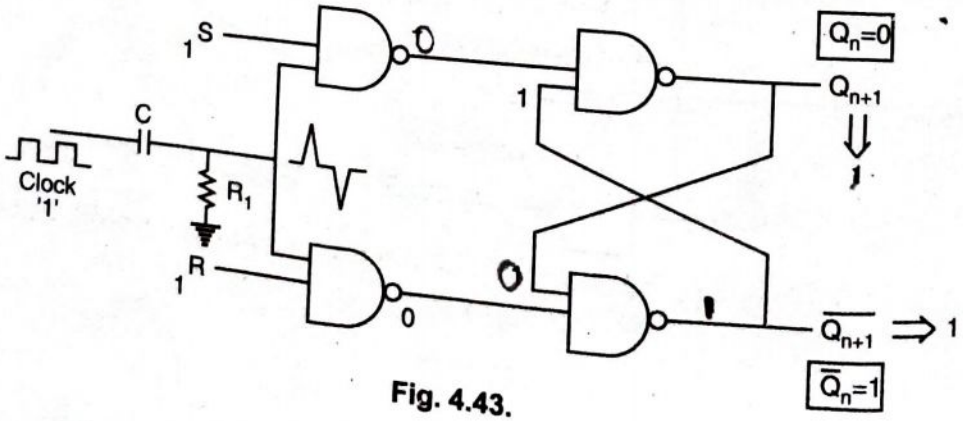


Fig. 4.43.

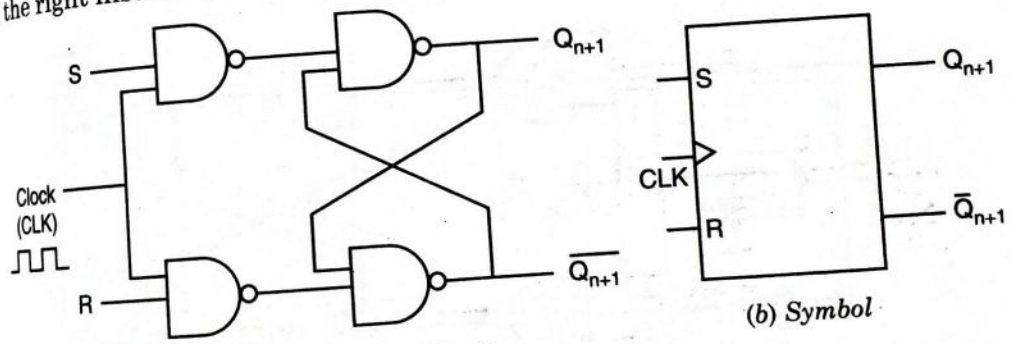
From case 4 : subcase 1 and subcase 2, we can conclude that, flip flop is said to be in indeterminate state.

The Truth table is given as follows :

Clock	S	R	Q_{n+1}
0	×	×	No change (Q_n)
1	×	×	No change (Q_n)
↓	×	×	No change (Q_n)
↑	0	0	Q_n
↑	0	1	0 (Reset)
↑	1	0	1 (Set)
↑	1	0	Indeterminate state

4.9 CLOCKED S-R FLIP FLOP

For clocked flip flop we provide extra input i.e., a square wave signal alongwith the inputs i.e., S and R. Clock signal (Clk) prevents the flip flop changing state till the right instant occurs. The circuit diagram is shown as :



(a) *Clocked S-R flip flop* (b) *Symbol*

Fig. 4.44.

Here where clock signal is '0', then there is no change in the output (it will remain in the previous state). When clock signal is high i.e., '1', then only output changes for different combinations of inputs.

i.e., — When clock = '1' and $S = 0$ & $R = 0$, then

Output $Q_{n+1} = Q_n$

– When clock = '1' and $S = 0$ & $R = 1$, then

Output $Q_{n+1} = 0$ (Reset state)

– When clock = 1 and $S = 1$ & $R = 0$, then

Output $Q_{n+1} = 1$ (Set state)

– When clock = 1, and $S = 1$ & $R = 1$, then

Output $Q_{n+1} = \overline{Q_{n+1}} = 1$ = Indeterminate state / Forbidden state.

Summarizing with Truth Table i.e.,

Clock (clk)	S	R	Q_{n+1}
0	×	×	No change (Q_n)
1	×	×	No change (Q_n)
1	0	0	Q_n (No change)
1	0	1	0 (Reset)
1	1	0	1 (Set)
1	1	1	Indeterminate state

'x' means don't care condition

4.10 EDGE TRIGGERED D-FLIP FLOP

Utility of D Flip Flop

To store single data bit i.e., either 1 or 0. D flip flop can be derived from S-R flip flop by adding an inverter in the circuit. Data input from S terminal is inverted and provided to R terminal.

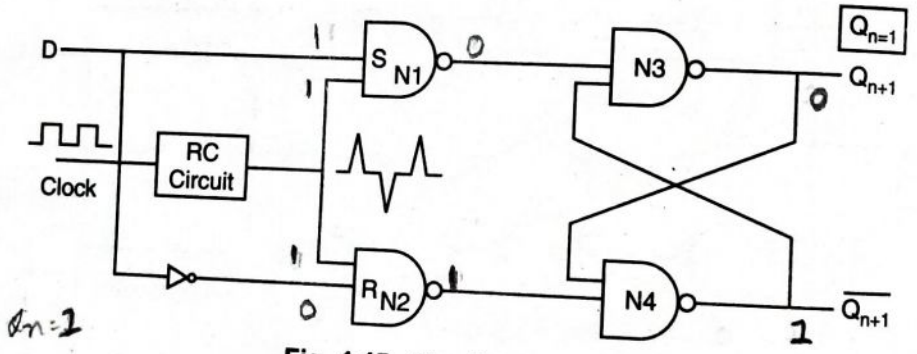


Fig. 4.45. Circuit Diagram.

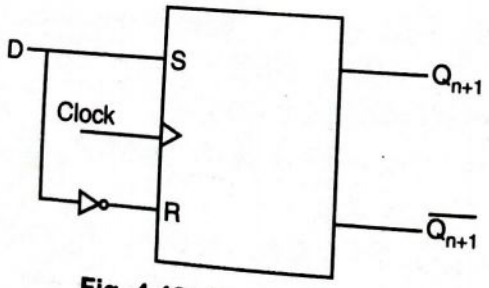
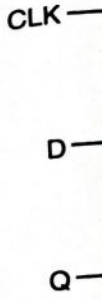


Fig. 4.46. Logic Symbol.

Timing Diagram of



Here

Timing Diagram

Timing Diagram of Positive Edge Triggered D Flip Flop

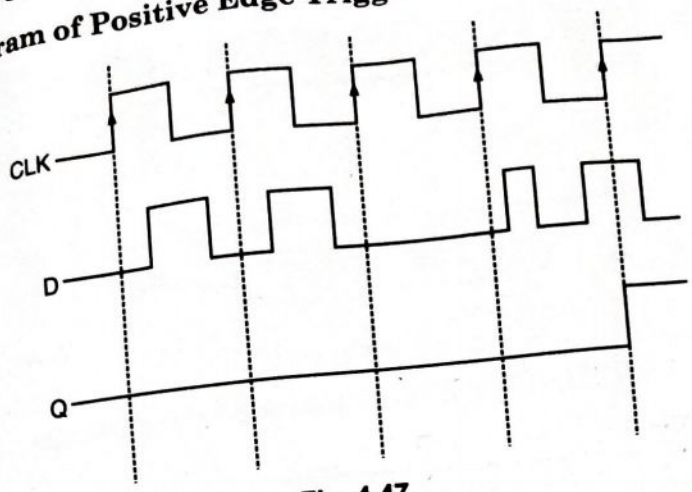


Fig. 4.47.

Here

CLK	D	Q
0	×	No change (NC)
1	×	No change (NC)
↓	×	No change (NC)
↑	0	0
↑	1	1

Timing Diagram For Clocked D Latch

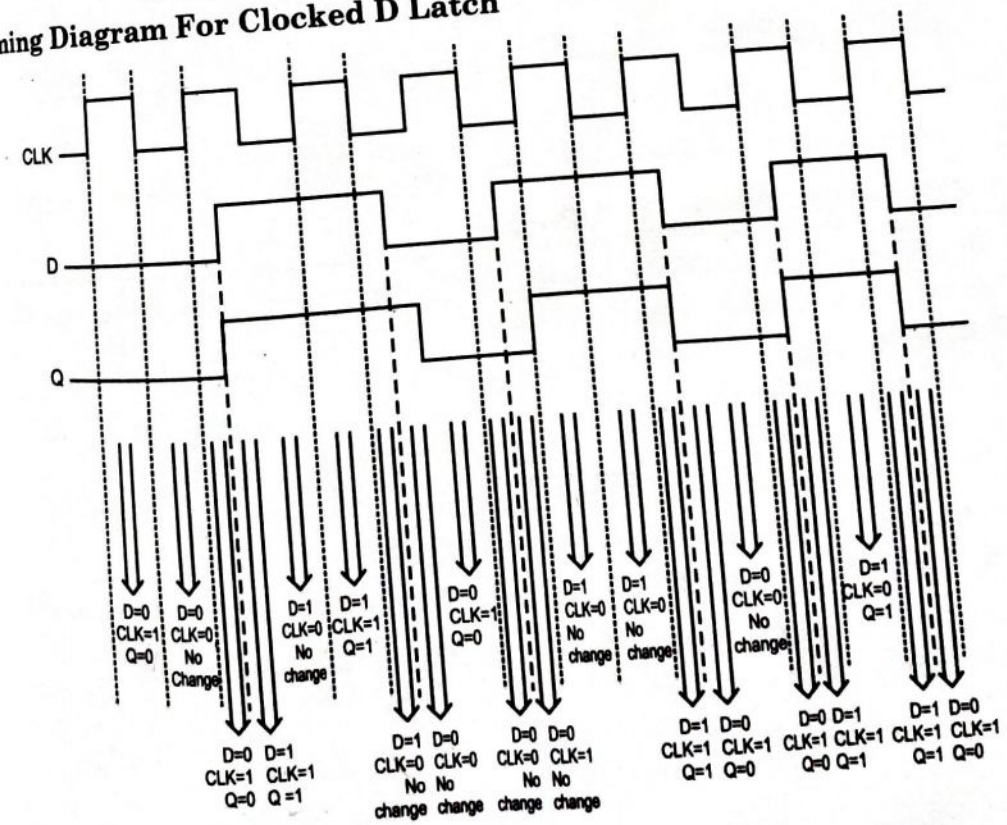


Fig. 4.48. (a)