In this case, we have two cross coupled NAND gates N_1 and N_2. Cross coupled means output of N_1 is connected as input of N_2 and similarly output of N_2 is connected as input of N_1. Due to this cross coupling, feedback is produced in the circuit and it is possible to attain either of two states 1 or 0.

DO YOU KNOW ?

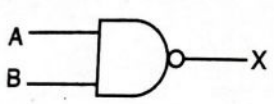
NAND and NOR Latches are preferred over Transistor Latches because of advancement of IC Technology.

Fig. 4.9 *S-R* Latch contains – Two Inputs – $\overline{S}$ & $\overline{R}$

– Two outputs – Q_{n+1} & $\overline{Q}_{n+1}$

where $\overline{Q}_{n+1}$ is complement of Q_{n+1}

As we are using NAND Gates, we must remember truth table of NAND Gate as :



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

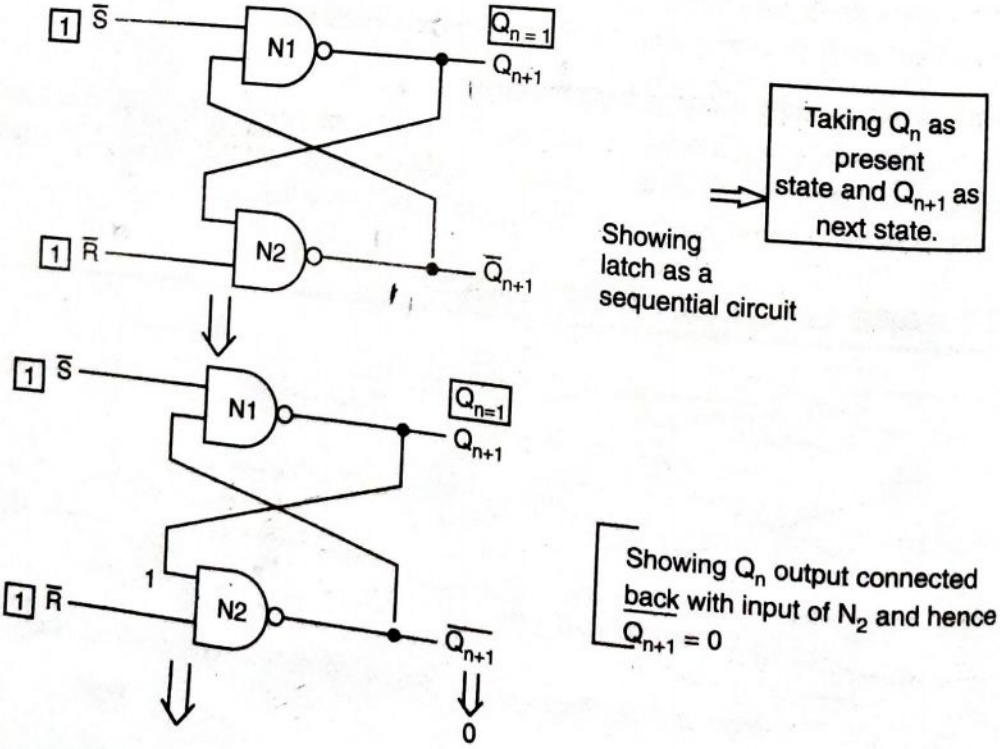
For NAND Gate,
If any input is low then output is high.
else output is low.

Fig. 4.11.

Taking different cases to explain functionality of NAND Latch :

Case 1 :

Assume $S = 0$, $R = 0$ Means $\overline{S} = 1$, $\overline{R} = 1$, $Q_n = 1$



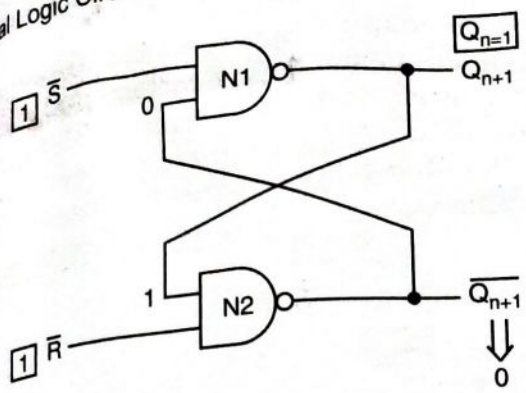


Fig. 4.12.

Concluding Case 1

Output $Q_{n+1} = 1$ is same as $Q_n = 1$ means Latch is in same state means no change in output. It is same as we had assumed.

Case 2 :

$S = 0$, $R = 1$ Means $\bar{S} = 1$, $\bar{R} = 0$

Assume $Q_n = 1$

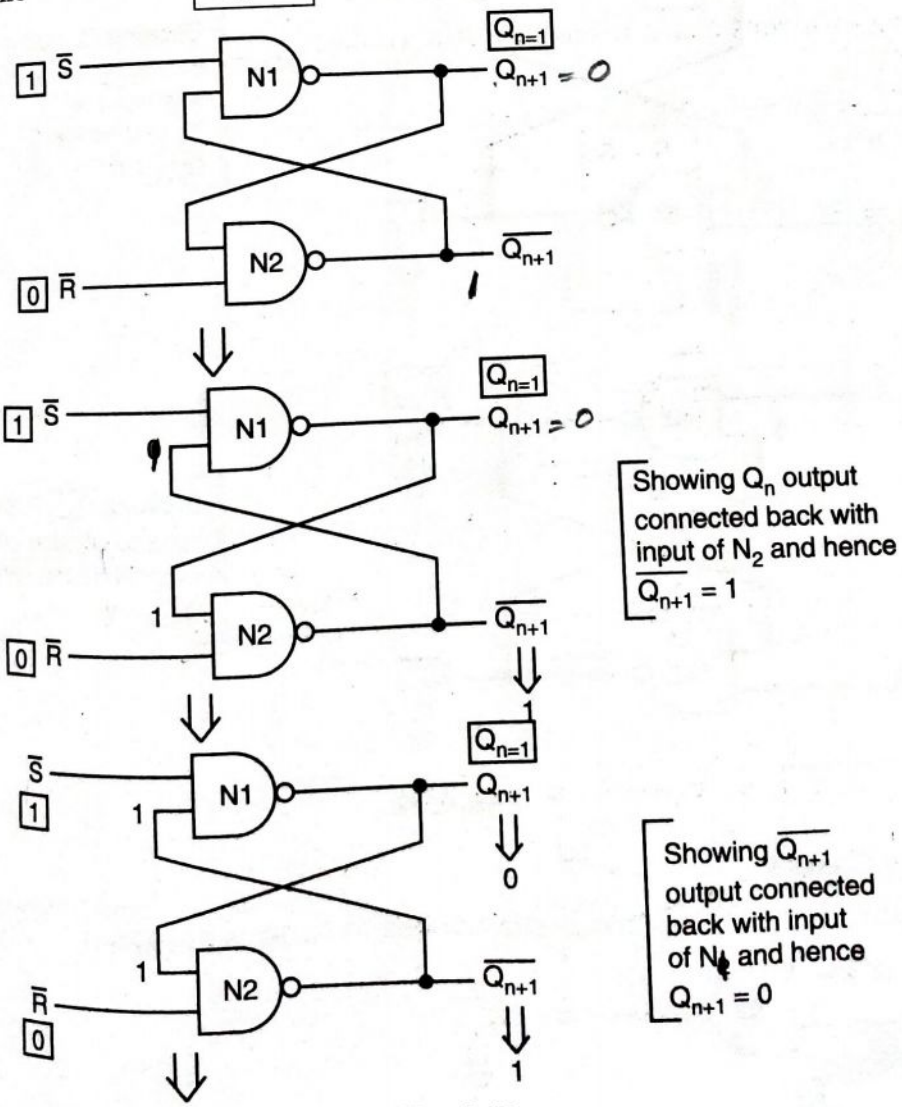


Fig. 4.13.

Concluding Case 2

As output $Q_{n+1} = 0$, Hence Latch is said to be in Reset or Clear state.

Case 3 :

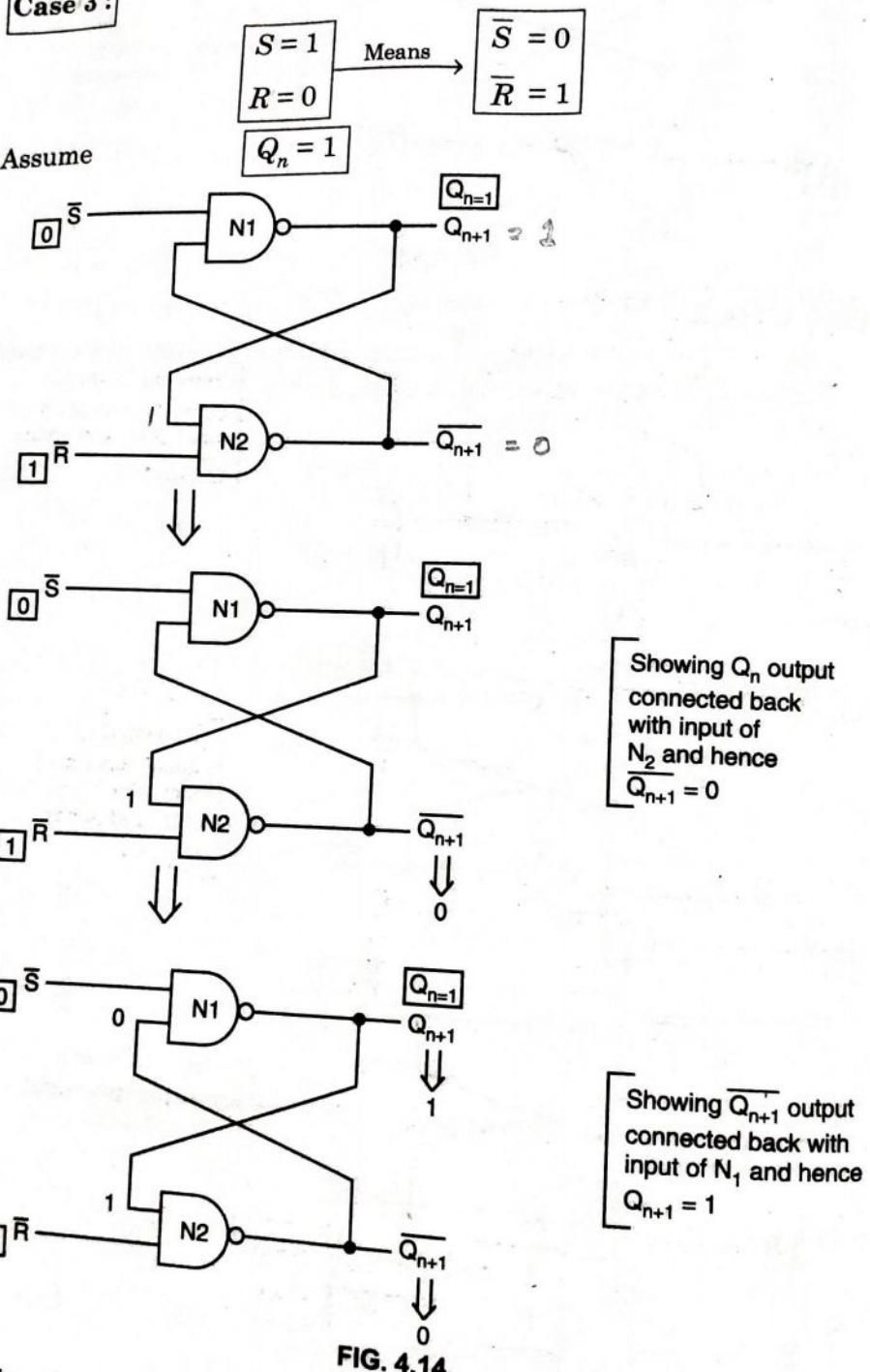
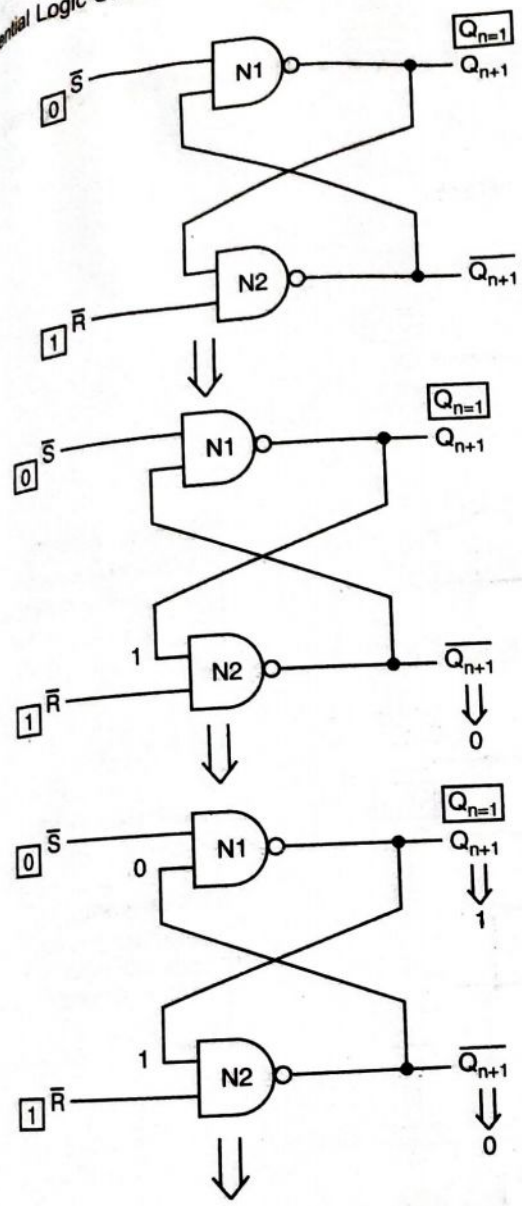


FIG. 4.14.

Concluding Case 3

As output $Q_{n+1} = 1$, Hence Latch is said to be in set state.



Showing Q_n output connected back with input of N_2 and hence $\overline{Q_{n+1}} = 1$

Showing $\overline{Q_{n+1}}$ output connected back with input of N_1 and hence $Q_{n+1} = 1$

Fig. 4.15.

Concluding Case 3 : As output $Q_{n+1} = 1$, hence latch is said to be in set state.

Case 4

S = 1, R = 1 Means $\bar{S} = 0$, $\bar{R} = 0$

Assume $Q_{n=1}$

S	R	$\bar{S}$	$\bar{R}$	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	1	1	0	0	1
0	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	0	1	1	1

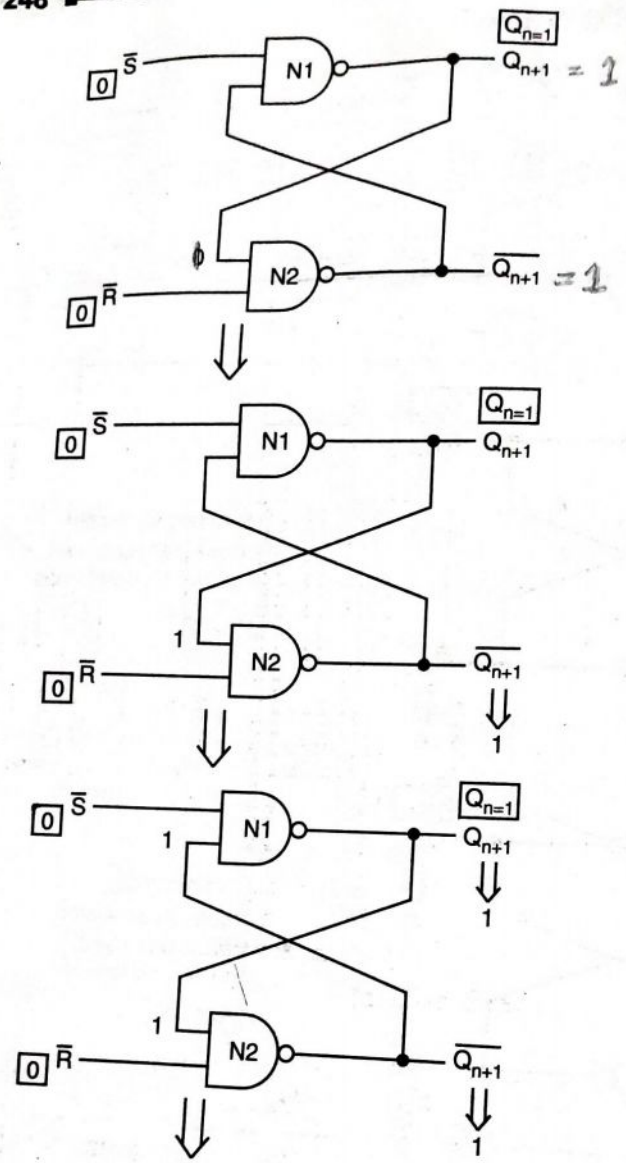


FIG. 4.16.

Concluding Case 4 : As $\overline{S} = \overline{R} = 0$, Both $Q_{n+1} = \overline{Q_{n+1}} = 1$. As $\overline{Q_{n+1}}$ is complement of Q_{n+1}, but we are getting both same and this is violating law of complement. Hence it is not allowed condition, that we have achieved.

Summarizing Four Cases

S	R	$\overline{S}$	$\overline{R}$	Q_{n+1}	$\overline{Q_{n+1}}$	State Achieved
0	0	1	1	Q_n	$\overline{Q_n}$	No Change (Inactive)
0	1	1	0	0	1	Reset (clear)
1	0	0	1	1	0	Set
1	1	0	0	?	?	Ambiguous/Forbidden State

4.4.1 Timing Diagram - NAND Latch

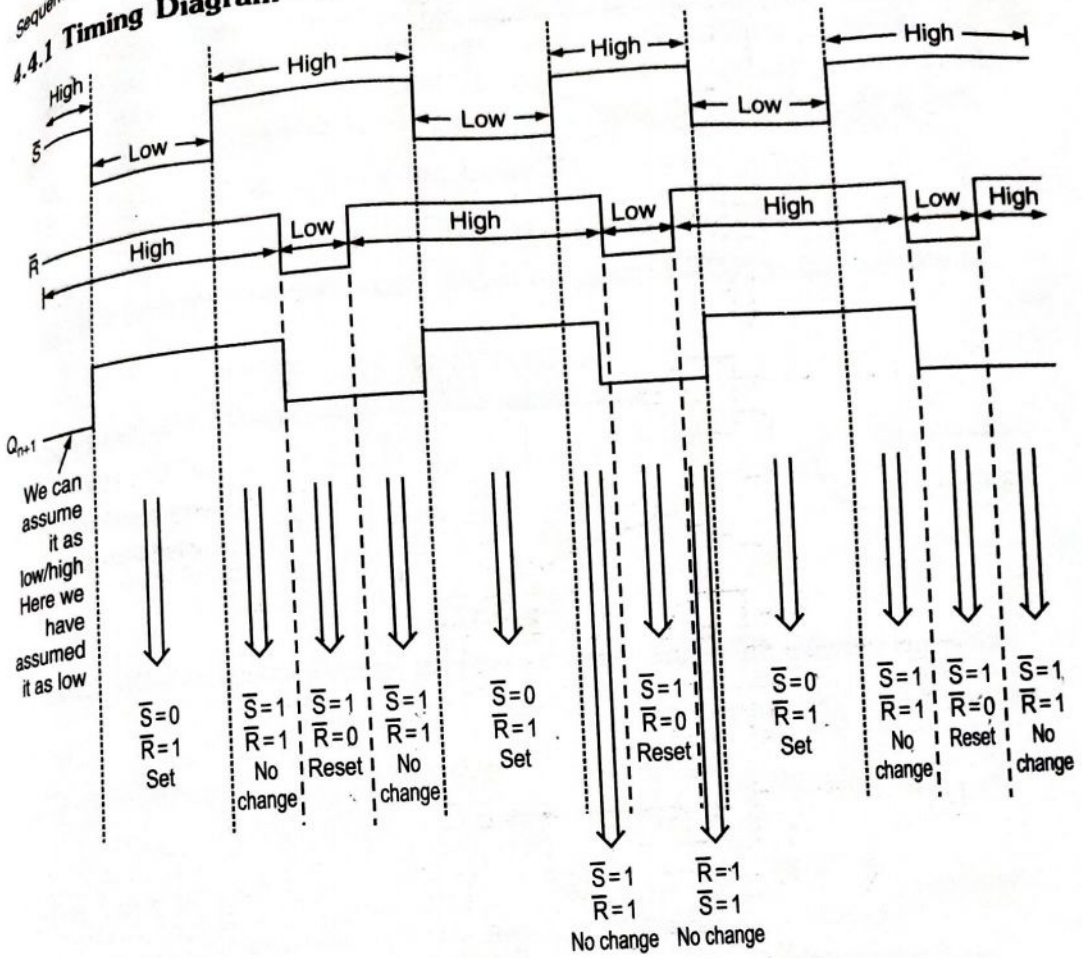


FIG. 4.16. (a)

Here

$\bar{S}$	$\bar{R}$	Q_{n+1}
0	0	Race/ Forbidden state
0	1	1 (Set)
1	0	0 (Reset)
1	1	No change

4.5 R-S NOR LATCH

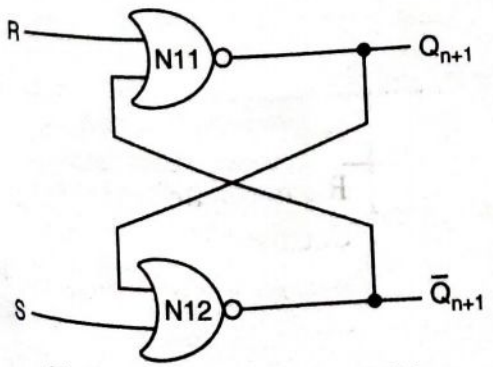


Fig. A. R-S Latch : Circuit Diagram.

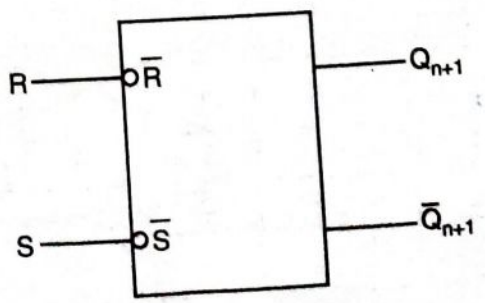


Fig. B. R-S Latch : Logic symbol

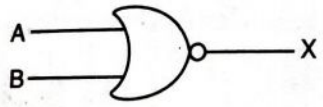
In this case, we have two cross coupled NOR gates N_{11} and N_{12}. Cross coupled means output of N_{11} is connected as input of N_{12} and similarly output of N_{12} is connected as input of N_{11}. Due to this cross coupling, feedback is produced in the circuit and it is possible to attain either of two states 1 or 0.

Fig. A : *S-R* Latch contains – Two Inputs – R & S as well as

– Two outputs – Q_{n+1} & $\overline{Q}_{n+1}$

where $\overline{Q}_{n+1}$ is complement of Q_{n+1}

As we are using NOR Gates, we must remember truth table of NOR Gate as :



A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

For NOR Gate,
If any input is high then output is low.
else output is high.

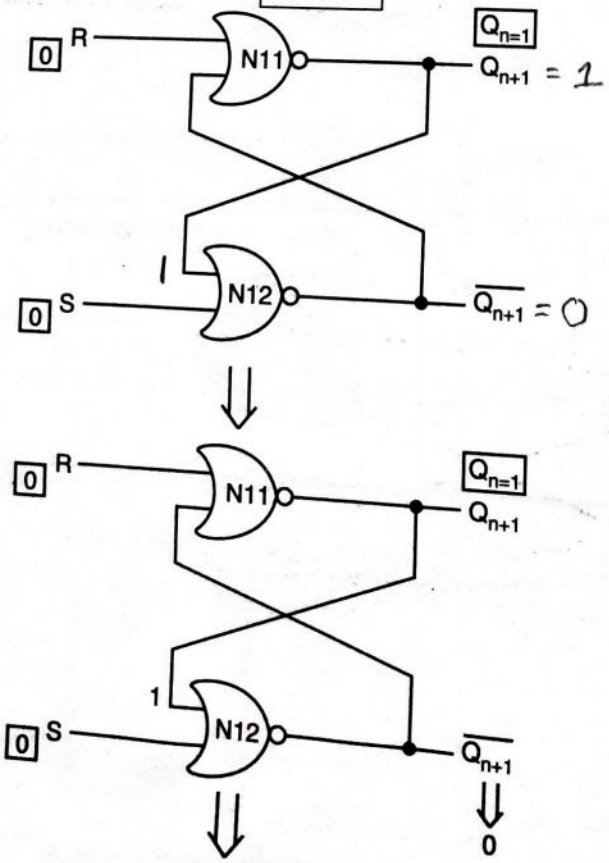
Fig. 4.17.

Let's again take different cases to explain functionality of NOR Latch :

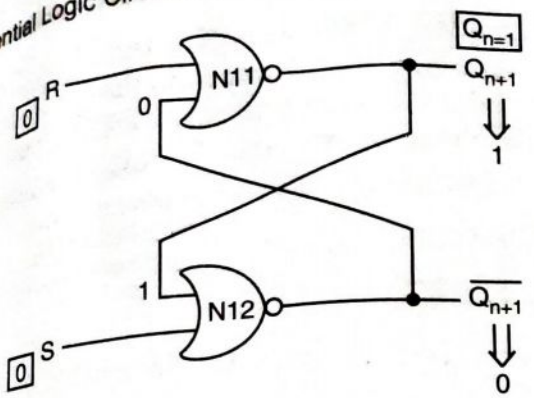
Case 1 : Subcase 1

$R = 0$
$S = 0$

Assume $Q_n = 1$



Showing Q_n output connected back with input of N_{12} and hence $\overline{Q_{n+1}} = 0$



Showing $\overline{Q_{n+1}}$ output connected back with input of N_{11} and hence $Q_{n+1} = 1$

FIG. 4.18.

Concluding Case 1 : Subcase 1 :

There is no change in output, as $Q_{n+1} = Q_n = 1$ (same). Hence this state is called as Inactive state.

Case 1 : **Subcase 2**

$R = 0$
$S = 0$

Assume $Q_n = 0$

Similar to subcase 1, we found that

$$Q_{n+1} = Q_n = 0$$

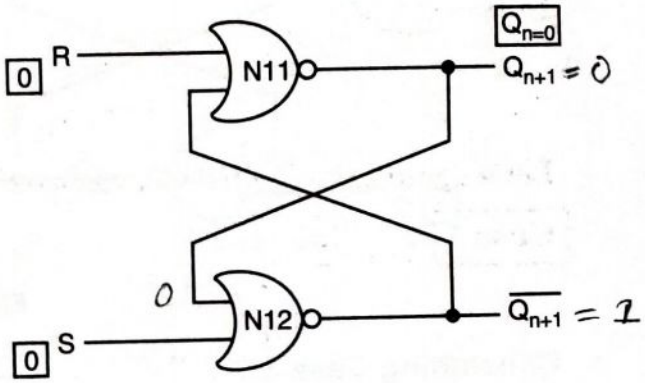


Fig. 4.19.

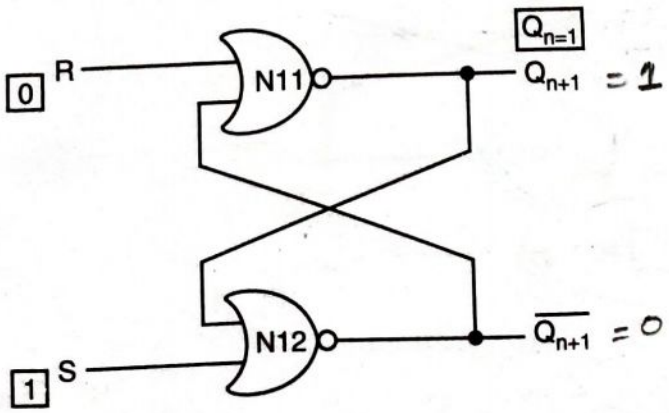
Concluding Case 1

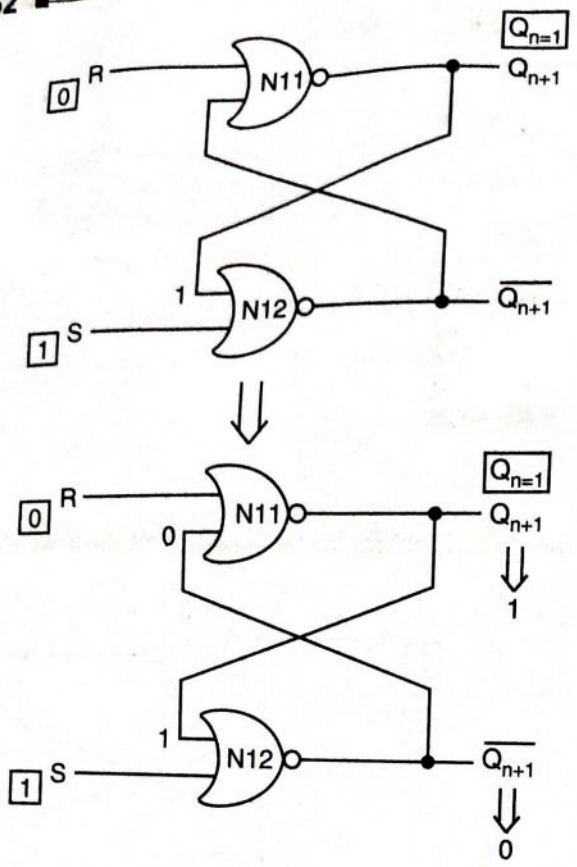
Output $Q_{n+1} = Q_n$ means Latch is in same state means no change in output. It is same as we had assumed.

Case 2 :

$R = 0$
$S = 1$

Assume $Q_n = 1$





Showing Q_n output connected back with input of N_{12} and hence $\overline{Q_{n+1}} = 0$

Showing $\overline{Q_{n+1}}$ output connected back with input of N_{11} and hence $\overline{Q_{n+1}} = 0$

Fig. 4.20.

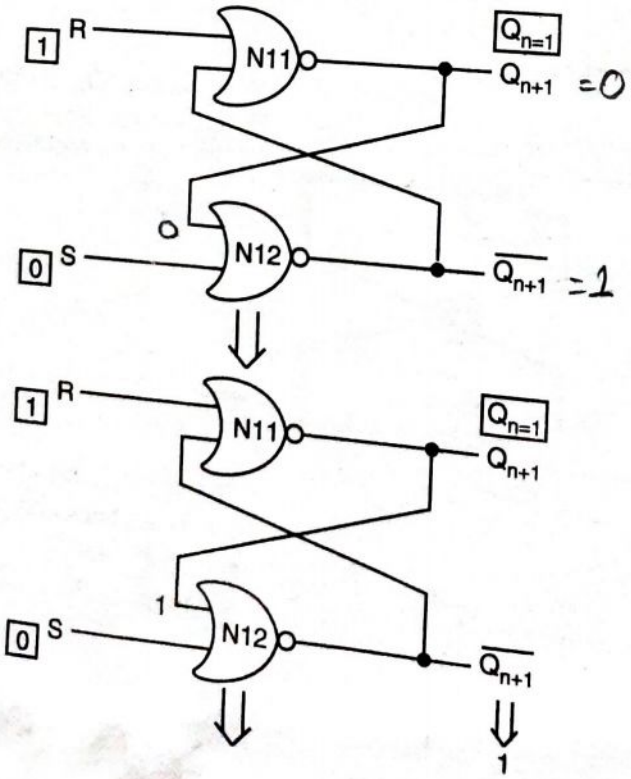
Concluding Case 2 :

As output $Q_{n+1} = 1$. Hence Latch is said to be in set state.

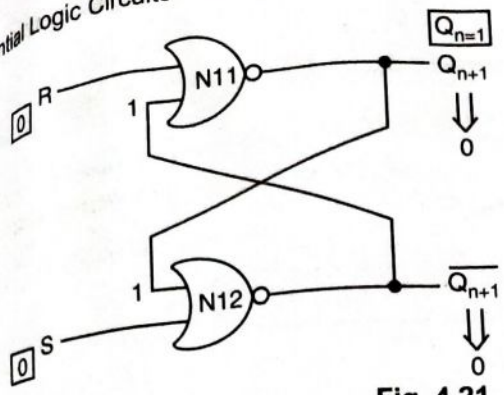
Case 3

$R = 1$
$S = 0$

Assume $Q_n = 0$



Showing Q_n output connected back with input of N_{12} and hence $\overline{Q_{n+1}} = 1$



Showing $\overline{Q_{n+1}}$ output connected back with input of N_{11} and hence $Q_{n+1} = 0$

Fig. 4.21.

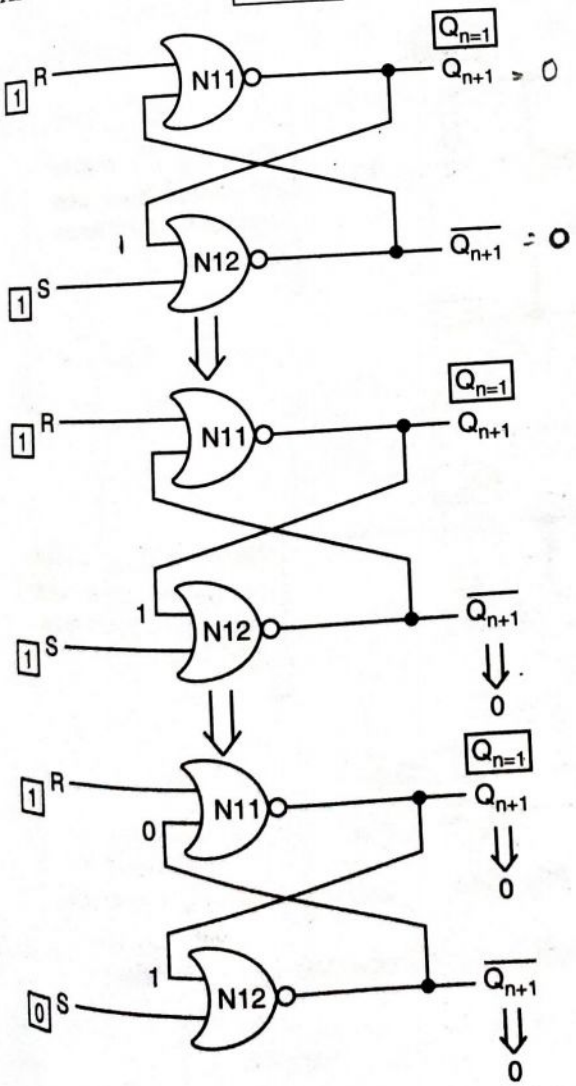
Concluding Case 3 :

As output $Q_{n+1} = 0$. Hence Latch is said to be in Reset or Clear state.

Case 4 : Subcase 1

$R = 1$
$S = 1$

Assume $Q_n = 1$



Showing Q_n output connected back with input of N_{12} and hence $\overline{Q_{n+1}} = 0$.

Showing Q_{n+1} output connected back with input of N_{11} and hence $\overline{Q_{n+1}} = 0$.

Fig. 4.22.

Concluding Case 4 : Subcase 1 :

Latch is said to be in invalid state or in Race condition because Q_{n+1} $\overline{Q_{n+1}}$ are simultaneously coming as 0.

Case 4 : Subcase 2

$R = 1$
$S = 1$

Assume $Q_n = 0$

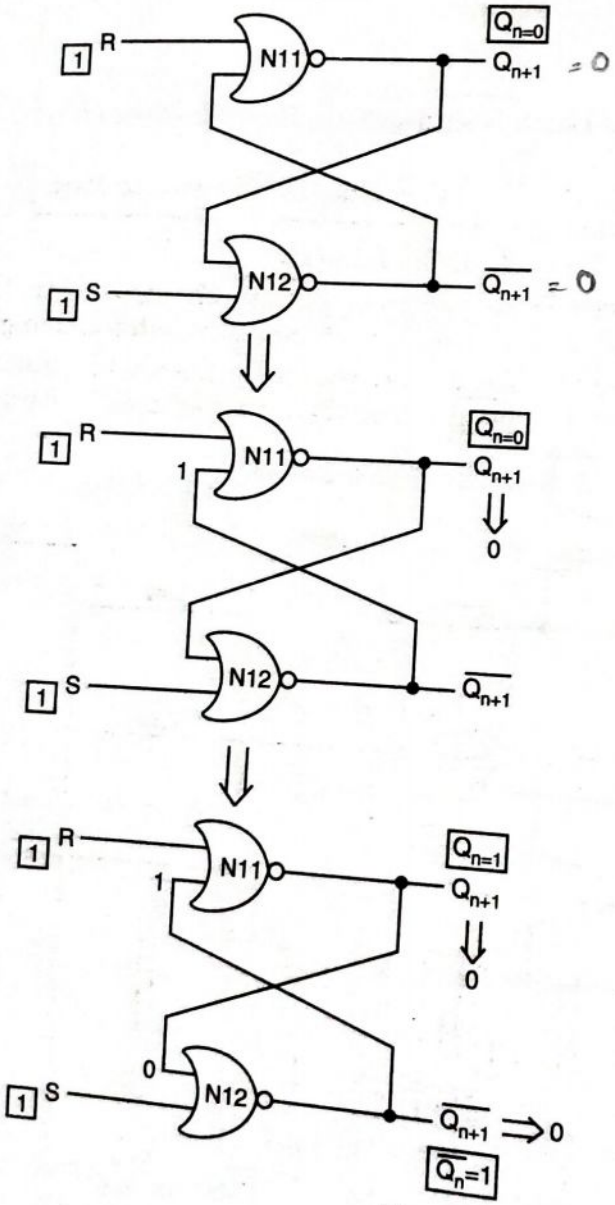


Fig. 4.23.

Again Latch is said to be in invalid state because $Q_{n+1} = \overline{Q_{n+1}} = 0$. Hence this condition must be avoided.

Sequential Logic Circui

Concluding Case

As Q and $\overline{Q}$ are '1' and violating the

Hence we never

Summarizing Fo

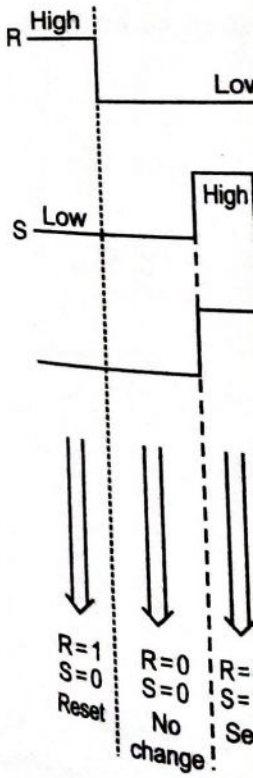
R	S
0	0
0	1
1	0
1	1

Comparison Bet

Nand Latch i one of the two app

NOR latch in one of the two app

4.5.1. Timing D



Concluding Case 4

As Q and $\overline{Q}$ are simultaneously coming as '0' or simultaneously coming as '1' and violating the fact that Q_{n+1} and $\overline{Q_{n+1}}$ are complement of each other. Hence we never apply $R = S = 1$, basically to avoid this condition.

Summarizing Four Cases

R	S	Q_{n+1}	$\overline{Q_{n+1}}$	State achieved
0	0	Q_n	$\bar{Q}_n$	No change
0	1	1	0	Set
1	0	0	1	Reset
1	1	?	?	Forbidden/Ambiguous or Race

Comparison Between NAND Latch & NOR Latch

Nand Latch inputs are normally 1 and there will be no change in output. If one of the two applied inputs is changed to 0, then the output of Latch is changed.

NOR latch inputs are normally 0 and there will be no change in output. If one of the two applied inputs is changed to 1, then the output of latch is changed.

4.5.1. Timing Diagram for R-S Latch (NOR Based)

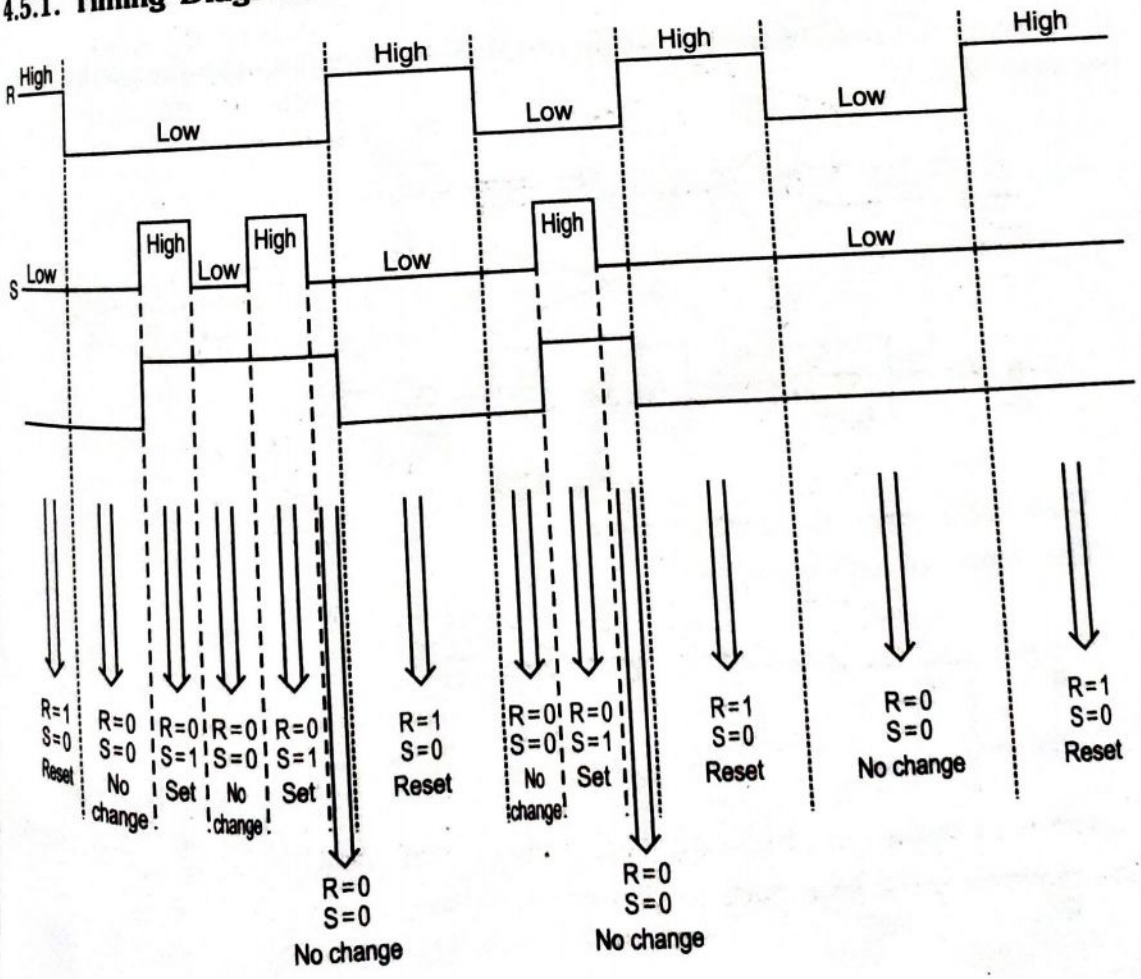


Fig. 4.24.

Here	R	S	Q_{n+1}
	0	0	No change
	0	1	1 (set)
	1	0	0 (Reset)
	1	1	Race

4.6 CLOCKED SR LATCH

The functionality of clocked SR-Latch is same on unclocked S-R latch but this synchronous sequential logic circuit. We are taking the case of a positive level triggered S-R Latch. Hence it must be clear that, this latch won't change its output until there is positive level of clock signal.

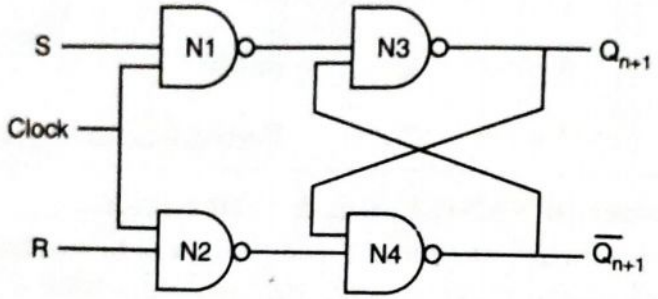


Fig. 4.25. Clocked S-R latch.

Let's take different cases to explain functionality of clocked S-R latch.

Case 1 $S = 0$, $R = 0$ & Clock = 0 & $Q_n = 0$

This is the case of initialization of latch and latch is assumed to be Reset because $Q_n = 0$.

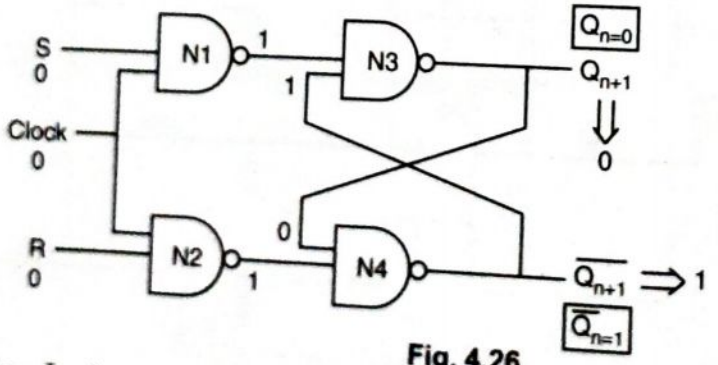


Fig. 4.26.

Now Let's make clock pulse high
This time we assume $Q_n = 1$.

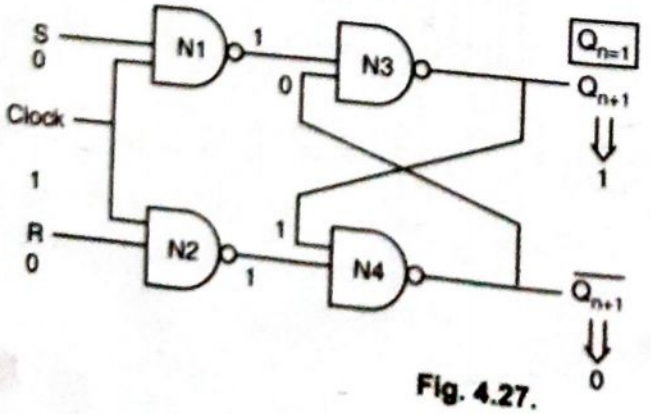


Fig. 4.27.

Case 2: $S = 1$, $R = 0$ & Clock-High & $Q_n = 1$

Subcase 1 :

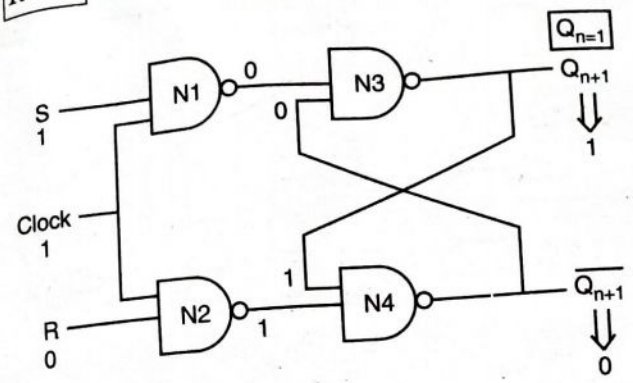


Fig. 4.28.

Let's reverse the situation and take $Q_n = 0$

Subcase 2 :

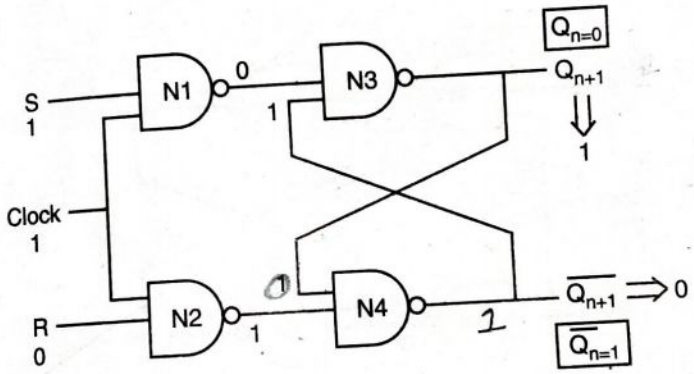


Fig. 4.29.

From case 2 : Subcase 1 & Subcase 2, we can conclude that Latch is in set state.

Case 3 $S = 0$, $R = 1$ & Clock-High & $Q_n = 1$

Subcase 1 :

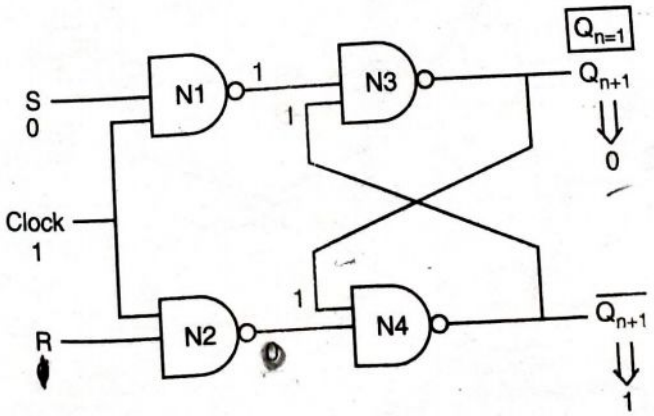


Fig. 4.30.

Let's reverse the situation and take $Q_n = 0$.

Subscase 2 :

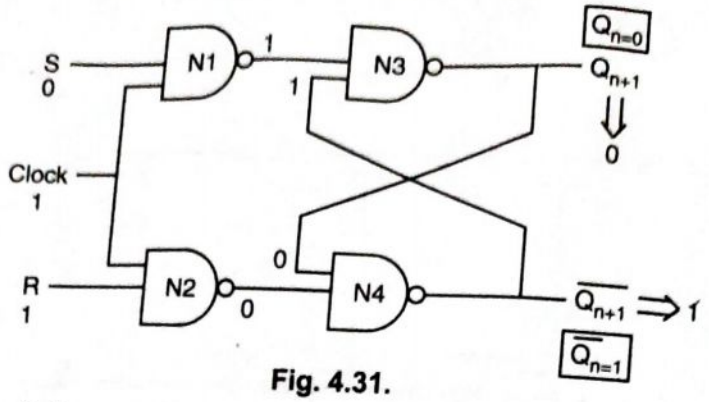


Fig. 4.31.

From case 3 : Subcase 1 & subcase 2, we can conclude that latch is in RESET or CLEAR state.

Case 4 $S = 1$, $R = 1$ & Clock-High & $Q_n = 1$

Subcase 1

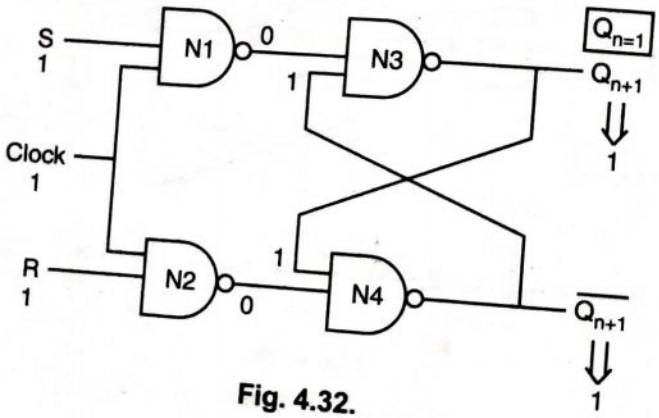


Fig. 4.32.

$Q_{n+1} = Q_{n+1} = 1$ [Voilating the statement that $\overline{Q_{n+1}}$ is complement of Q_{n+1}]

Let's reverse the situation and take $Q_n = 0$.

Subcase 2

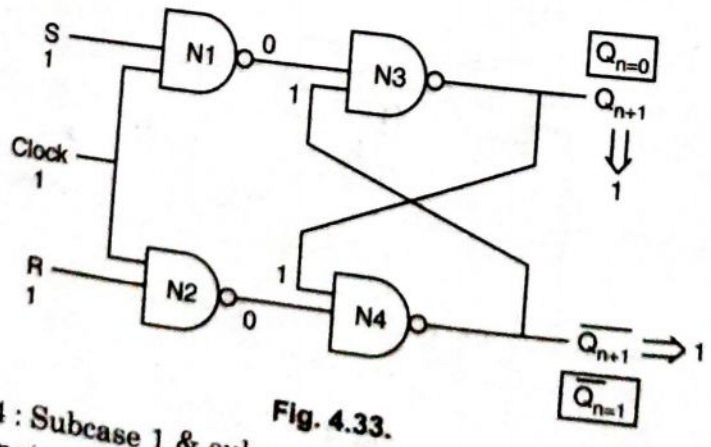


Fig. 4.33.

From case 4 : Subcase 1 & subcase 2, we can conclude that, latch is said to be in indeterminate state.

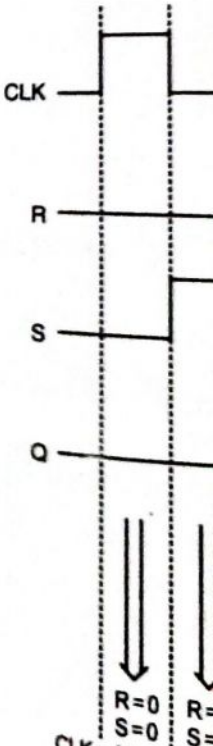
Sequential Logic

Summari

Clk	
0	
1	
1	
1	
1	
1	

Clk	
1	
1	
1	
1	

4.6.1. Timin



Summarizing with Truth table

Clk	S	R	Q_{n+1} $\overline{Q_{n+1}}$
0	×	×	No Change
1	×	×	No Change
1	0	0	Q_n $\overline{Q_n}$
1	0	1	0 (Reset) 1
1	1	0	1 (Set) 0
1	1	1	Indeterminate state / Forbidden state

Or

Clk	S	R	Q_{n+1}
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Forbidden state

4.6.1. Timing Diagram Clocked S-R Latch

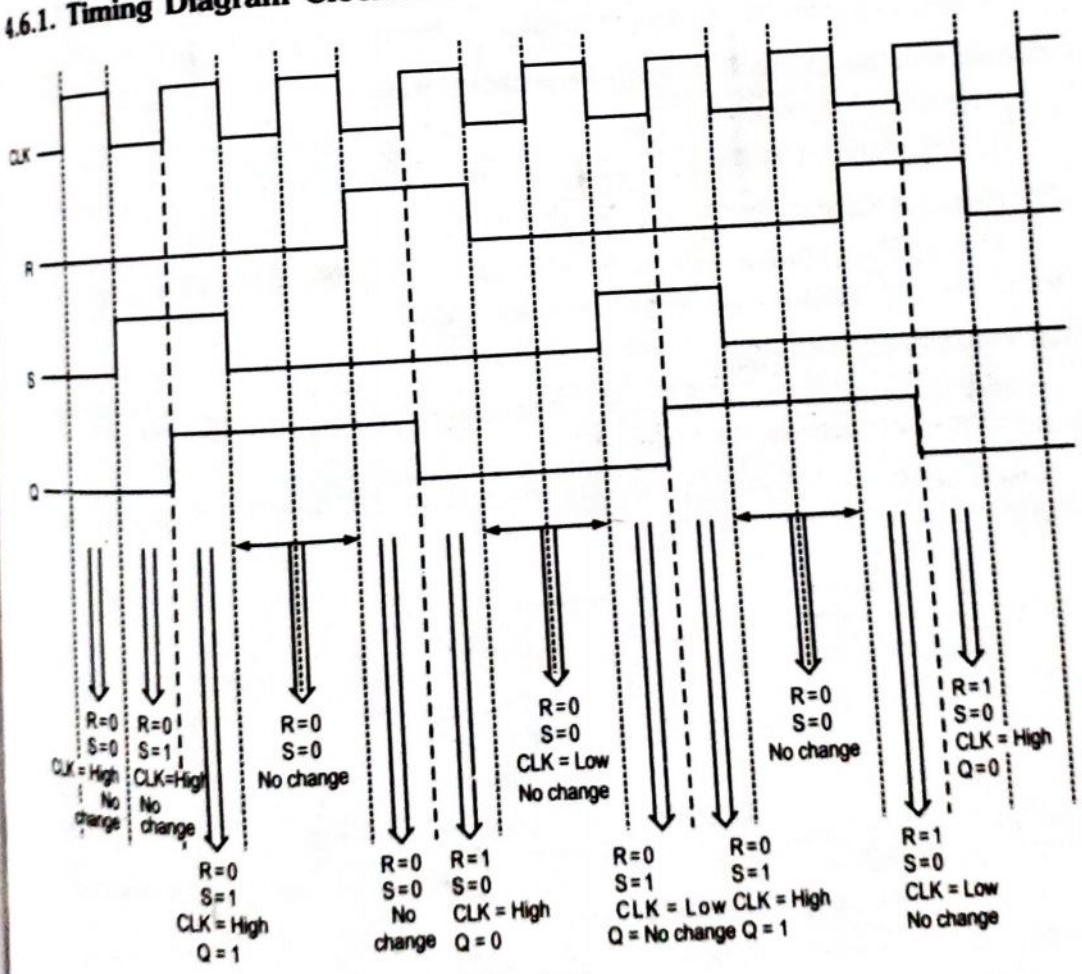


Fig. 4.34.