4 SEQUENTIAL LOGIC CIRCUITS AND ITS DESIGN

4.1. INTRODUCTION

There are two types of Logic Circuits :

(1) Combinational Logic Circuits

(2) Sequential Logic Circuits

(1) Combinational Logic Circuits

In these circuits, output depends only on the present input values.

For example : Let us consider an XNOR gate as an combinational circuit.

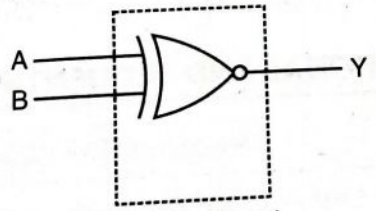


Fig. 4.1.

The output Y is always depends on the present state of A, B *i.e.* the present input.

(2) Sequential Logic Circuits

In these circuits, output can depend on past as well as present input values.

Sequential circuits are the circuit in which memory element is present. Memory element is capable of storing binary digits '0' or '1'.

For example : Let us consider an sequential circuit which is formed by combining memory element and the combinational circuit.

In This Chapter

Inside this Chapter

- Latch
- SR flip flop
- JK flip flop
- Classification of flip flop
- Race around condition
- Master slave JK Flip flop
- D flip flop
- T flip flop
- Conversion of one Flip flop to another
- Counter
- Register
- Shift register
- Universal shift register
- Bidirectional shift register
- Comparison between Latch and flip flop
- Comparison between Ring and Johnson counter
- Designing of sequential circuits
- Excitation table
- Designing of Modulus counter
- Designing of Asynchronous (Ripple) counter

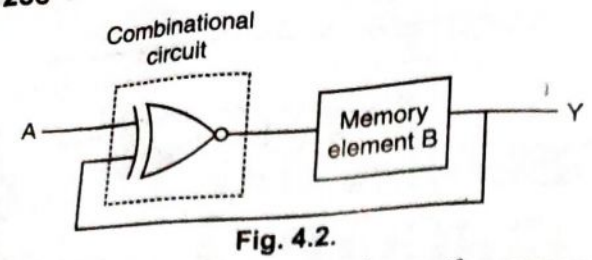


Fig. 4.2.

The value of Y is depends on the present value of A and past value of A.

Let us assume memory element, B hold the initial value zero ('0'). Now if the value of A is 0 there output become 1 and then the value of A is changed to 1 then output is 1. Hence the value of output Y is depends on present and past value of input A.

Sequential Logic Circuits are of two types :

(1) Synchronous/clocked sequential logic circuits.
(2) Asynchronous/unclocked sequential logic circuits.

(1) Synchronous/Clocked Sequential Logic Circuits

In these circuits, event occurs in synchronization with clock pulse. As event is allowed to occur only with synchronization with clock pulse, hence this makes system very much stable, as demanded by latest technology.

(2) Asynchronous Sequential Logic Circuits

In these circuits, event occurs without any synchronization with clock pulse. Any event can occur just after combination of another event and hence it does not wait for clock pulse. This makes system unstable.

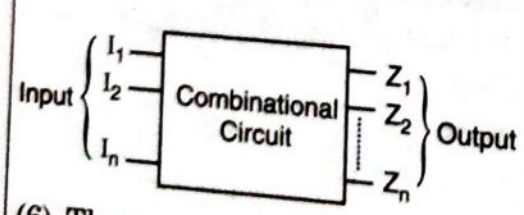
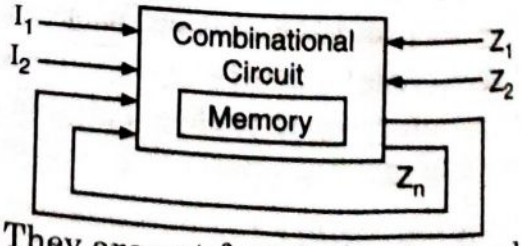
DO YOU KNOW ?

Combinational circuits are faster than sequential circuits because these circuts don't have memory.

DO YOU KNOW ?

Asynchronous sequential logic circuits are faster than synchronous sequential logic circuits.

4.2 COMPARISON BETWEEN COMBINATIONAL AND SEQUENTIAL CIRCUITS

Combinational Circuits	Sequential Circuits
(1) In these circuits output depends only on the present input values.	(1) Output can depend on past as well as present input values.
(2) They do not have memory.	(2) They do have memory.
(3) No feedback is present	(3) Feedbacks are present.
(4) It is specified by a set of Boolean function.	(4) The outputs are a function of the current inputs and the state of memory elements (past inputs)
(5) It is represented as 	(5) It is represented as 
(6) They are faster than sequential circuit.	(6) They are not fast due to feedback action.
(7) Examples of combinational circuits are Address, Multiplexers, Subtractors etc.	(7) Examples of sequential circuits are : Flip-flops, Counters, Registers etc.

4.3 LATCH

Latch is a bistable device. Bistable device means it can attain two states either 1 or 0 with the help of feedback arrangement associated with it. As one bit of information can be locked by this bistable sequential device. Hence it is called as latch. In technical terms, Latch is also known as memory element to store one bit of information – either 1 or 0.

DO YOU KNOW ?

Because of feedback arrangement, latch is also called as sequential circuit.

We can make circuit of Latch by using two cross coupled transistors as shown below :

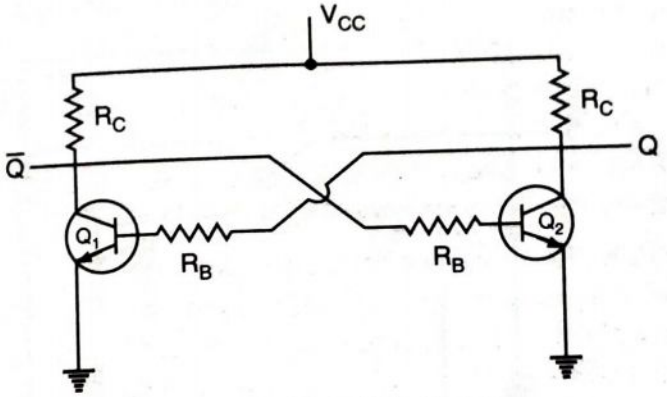


Fig. 4.3. Transistor Latch

In this diagram, we have two cross coupled transistors Q_1 and Q_2. The output of Q_2 drives input of Q_1 through resistance R_B. Similarly the output of Q_1 drives input of Q_2 through resistance R_B.

Q_1 and Q_2 are taken as two similar transistors in terms of their manufacturing, operation and characteristics.

Let's take two cases to explain operation of Transistor Latch :

Case 1 : If Q_1 is saturated, then $V_{CE} = 0$, means no base current for transistor Q_2. Because output of Q_1 is driving Q_2. Hence Q_2 goes to cut off state. Hence output of $Q_2 = V_{CC}$. This high voltage at output of Q_2 produces enough base current to drive input of Q_1. In this way Q_1 is sustained in its saturation state and output Q for the overall circuit is approximated as V_{CC}.

Case 2 : If Q_2 is saturated, then no base current for transistor Q_1. Because output of Q_2 is driving Q_1. Hence Q_1 goes to cut off state. Hence output of $Q_1 = V_{CC}$. This high V_{CC} produces enough base current to drive input of Q_2. In this way Q_2 is sustained to work in saturation and output of overall circuit is Q is approximately equal to 0 V.

Concluding case 1 and case 2.

The overall circuit is said to be latched.

Case 1 Summary — "Circuit is latched and storing logic 1."

Case 2 Summary — "Circuit is latched and storing logic 0."

Limitation of Above Circuit

This circuit is not suitable for getting desired digital information. When power is switched on, then this circuit automatically switches to one of the two stable states either 1 or 0 and that state is unpredictable.

To avoid above limitation, we can switch over to controlled transistor latch.

4.3.1. Controlled Transistor Latch

If we take two inputs to simple transistor latch. Then we can control this latch. These control inputs can be assigned any value either 1 or 0. The circuit diagram for controlled transistor latch is shown below :

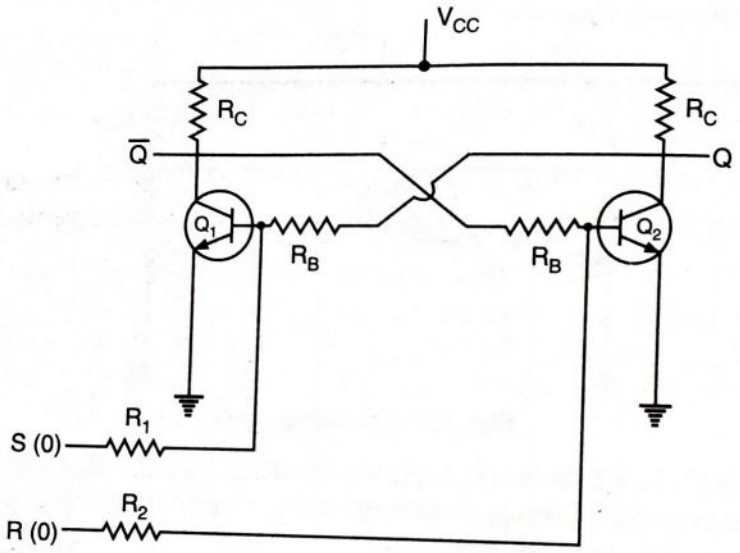


Fig. 4.4.

Case 1 : $R = 0$

$S = 0$

Let's assume $Q = 1$

As $Q = 1$, Hence Q is coupled back to input of Q_1. It means Q_1 – ON. The output of $Q_1 = 0$ is coupled to input of Q_2. In this way Q_2 will be OFF and hence output of $Q_2 = 1$.

In this way $Q = 1$, means no change in output. Output is same as that we have assumed.

Case 2 : $R = 0$

$S = 0$

Let's assume $Q = 1$

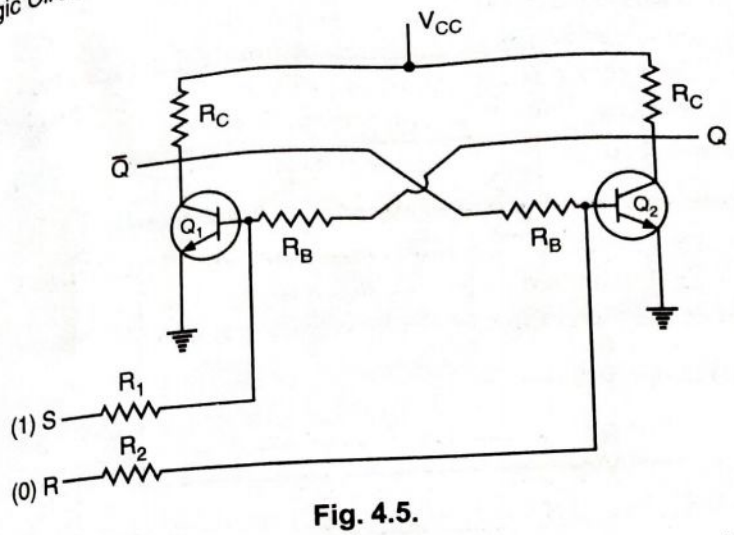


Fig. 4.5.

High S forces the transistor Q_1 to saturate. If Q_1 is in saturation state, then output of overall circuit is obtained as logic 1. It means circuit is said to be latched and logic 1 is stored.

Case 3 : $R = 1$

$S = 0$

Let's assume $Q = 1$

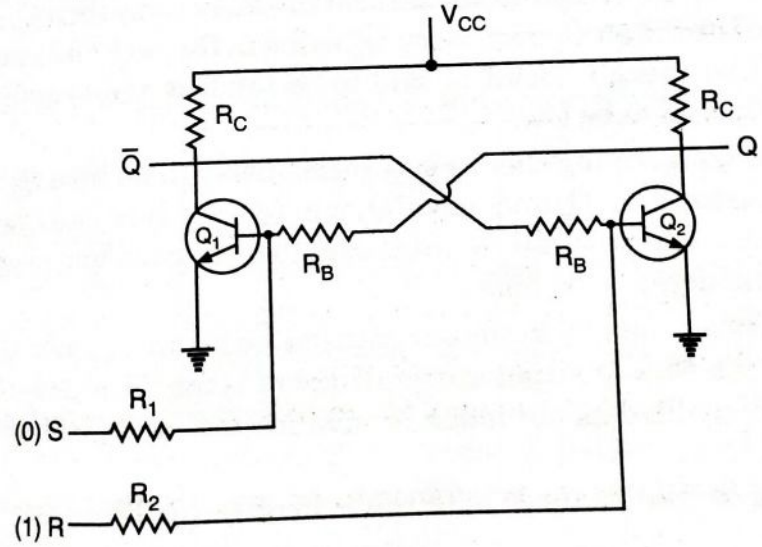


Fig. 4.6.

High R forces the transistor Q_2 to saturate. If Q_2 is in saturation, then output of overall circuit is obtained as logic 0. It means circuit is said to be latched and logic 0 is stored.

Case 4 : $R = 1$

$S = 1$

Let's assume $Q = 1$

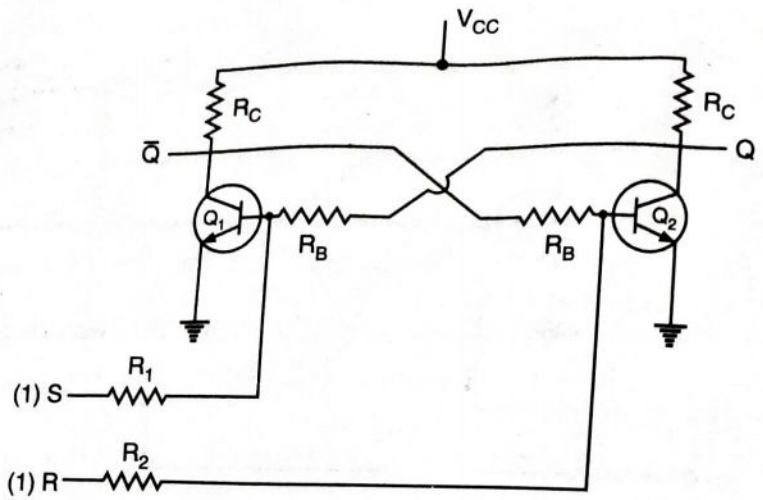


Fig. 4.7.

If $R = S = 1$, then Q_1 and Q_2 transistors are forced to saturation.

Suddenly if R and S are returned to low, then both transistors try to come out of saturation. It will depends on saturation delay time of Q_1 and Q_2 to come out of saturation.

Let's take two cases :

Case 1 : If Q_1 is having shorter saturation delay time, then Q_1 is considered as faster transistor than Q_2 and hence Q_1 will win the race and first come out of saturation. Then overall circuit is said to be latched and overall output Q of circuit is considered to be low.

Case 2 : If Q_2 is having shorter saturation delay time, then Q_2 is considered as faster transistor than Q_1 and hence Q_2 will win the race and first come out of saturation. Then again overall circuit is said to be latched and overall output Q of circuit is considered to be high.

But we have assumed two similar transistors means Q_1 and Q_2 are equally considered as fast. Now Q output of overall circuit is considered as unpredictable. This state is also called as forbidden or invalid state and generally avoided in digital circuits.

Concluding overall analysis with the help of Truth Table as :

R	S	Q
0	0	No change
0	1	Set (1)
1	0	Reset (0)
1	1	Race (*)

We can construct Latch circuit by using cross coupled NOT Gates, NAND Gates or NOR Gates.

Let's make circuit of a basic latch by using two cross coupled NOT Gates (Inverters) :

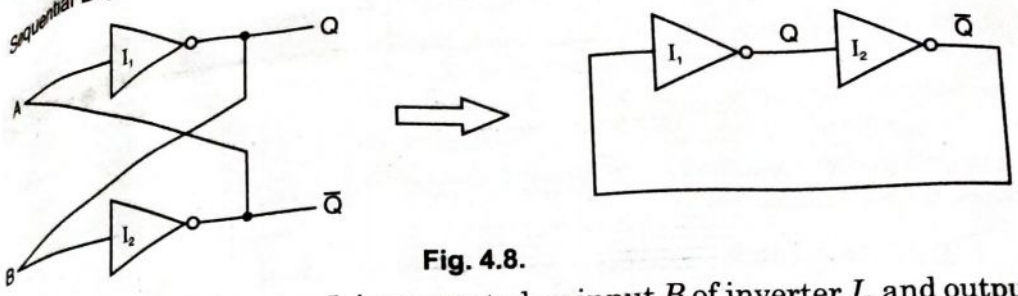


Fig. 4.8.

The output Q of inverter I_1 is connected as input B of inverter I_2 and output $\bar{Q}$ of inverter I_2 is coupled as input A of inverter I_1. This type of connection is most commonly known as cross coupling.

Case 1 : Let's take $Q = 1$

Now $Q = B = 1$ means input of $I_2 = 1$. Hence output of inverter I_2 i.e., $\bar{Q} = 0$. So we get input of inverter I_1 i.e., $A = 0$. Hence output of inverter I_1 i.e., $Q = 1$

$$\boxed{A = 0, \quad B = 1, \quad Q = 1, \quad \bar{Q} = 0}$$

Case 2 : Let's take $Q = 0$

Now $Q = B = 0$ means input of $I_2 = 0$. Hence output of inverter I_2 i.e., $\bar{Q} = 1$. So we get input of inverter I_1 i.e., $A = 1$. Hence output of inverter I_1 i.e., $Q = 0$

$$\boxed{A = 1, \quad B = 0, \quad Q = 0, \quad \bar{Q} = 1}$$

We found that Q and $\bar{Q}$ are complementing of each other : means if $Q = 1$, then $\bar{Q} = 0$ and else $Q = 0$, then $\bar{Q} = 1$.

Limitation of Logic Circuit

This circuit is not suitable for getting desired digital information when this circuit is switched on, then circuit automatically switches to one of the two stable states, either 1 or 0 and that state is unpredictable.

Remedy to Remove above Limitation

We modify this latch with provision to enter desired digital information by replacing two cross coupled inverters with either two cross coupled NAND gates (two-input) or two cross coupled NOR gates (two-input).

4.4 S-R NAND LATCH (SET-RESET LATCH)

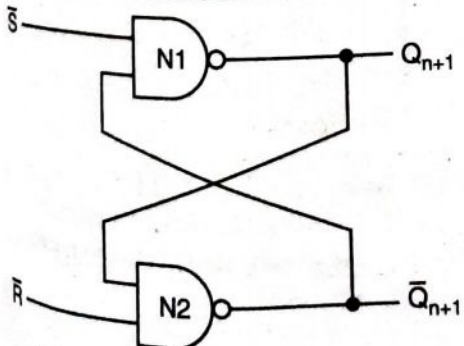


Fig. 4.9. S-R Latch : Circuit Diagram.

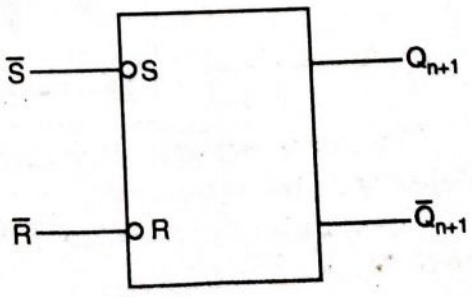


Fig. 4.10. S-R Latch : Logic symbol