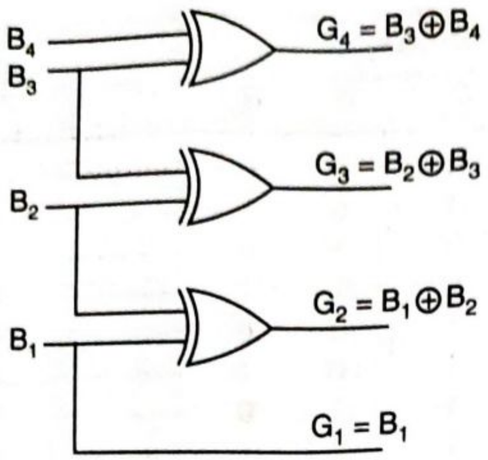

Fig. 3.59. Circuit Diagram for Binary to Gray Code Decoder

3.20 MAGNITUDE COMPARATOR

Magnitude comparator is one of the useful combinational logic networks and has wide application. It compares two binary numbers and determines one number is greater than, less than or equal to the other number. It is a multiple output combinational logic circuit. If two binary numbers are considered as A and B, the magnitude comparator gives three output for $A > B$, $A < B$ and $A = B$.

The comparator will do the comparison from the most significant bit (i.e. A_3 and B_3), then result is $A > B$. If the MSB's are equal, then next bit *i.e.* A_2 and B_2 is compared and so on until the least significant bit is reached.

1-Bit Comparator Circuit

For 1-bit circuit only two bits are there *i.e.* $0 < 1$. The truth table for 1-bit is given as follows :

Inputs		*Outputs*		
A	***B***	***A > B***	***A = B***	***A < B***
0	0	0	1	0
1	0	1	0	0
0	1	0	0	1
1	1	0	1	0

For Bit $A = 0$ and $B = 0$, the output is $A = B$, hence output corresponding to $A = B$ is high and rest two outputs $A > B$ and $A < B$ is low. Similarly for $A = 1$ and $B = 1$, output $A = B$ is high and for $A = 1$ and $B = 0$, output $A > B$ is high and for last combination *i.e.* $A = 0 < B = 1$, $A < B$ output bit is high.

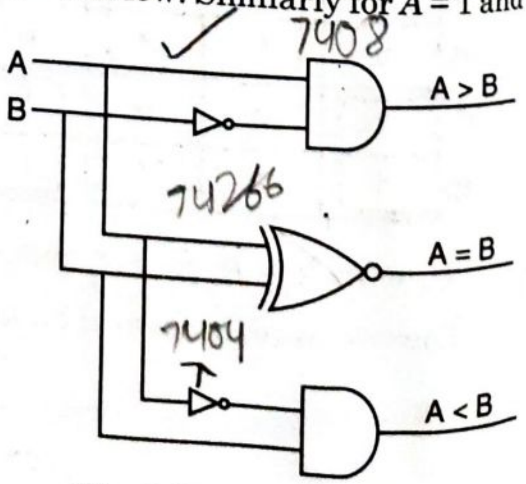

Fig. 3.60. Designing of 1-bit Comparator.

Designing of 1-bit Comparator

For
$$A > B$$

Output expression is given as $\Rightarrow A\bar{B}$

For
$$A = B$$

$$\text{Output} = \bar{A}\,\bar{B} + AB$$

For
$$A < B$$

$$\text{Output} = \bar{A}B$$

2-Bit Comparator

For 2-bit comparator the truth table is given as follows :

Let us represent the input A by two bits *i.e.* $A_0\,A_1$ and input B by $B_0\,B_1$. The outputs are $A > B$, $A < B$ and $A = B$. The outputs are obtained by comparing the bits A_0, B_0, A_1 B_1.

The truth table is as follows :

	Inputs				***Outputs***		
	A_0	A_1	B_0	B_1	$A > B$	$A = B$	$A < B$
0	0	0	0	0	0	1	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	0	1
3	0	0	1	1	0	0	1
4	0	1	0	0	1	0	0
5	0	1	0	1	0	1	0
6	0	1	1	0	0	0	1
7	0	1	1	1	0	0	1
8	1	0	0	0	1	0	0
9	1	0	0	1	1	0	0
10	1	0	1	0	0	1	0
11	1	0	1	1	0	0	1
12	1	1	0	0	1	0	0
13	1	1	0	1	1	0	0
14	1	1	1	0	1	0	0
15	1	1	1	1	0	1	0

The K-map realization for $A > B$, $A = B$ and $A < B$ is given as follows :

$B_0 B_1 \backslash A_0 A_1$	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

$A > B = A_0\overline{B_0} + A_1\,\overline{B_0}\,\overline{B_1}$
$+ \overline{B_1}\,A_0 A_1$

$B_0 B_1 \backslash A_0 A_1$	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

$A = B \Rightarrow \overline{A_0}\,\overline{A_1}\,\overline{B_0}\,\overline{B_1} + \overline{A_0}\,A_1\,\overline{B_0}\,B_1 +$
$A_0\,A_1\,B_0\,B_1 + A_0\overline{A_1}\,B_0\overline{B_1}$

$B_0 B_1 \backslash A_0 A_1$	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

$A > B = \overline{A_0}\,B_0 + \overline{A_0}\,\overline{A_1}\,\overline{B_1} + \overline{A_1}\,B_0\,B_1$

Circuit Designing is shown in figure 3.61, 3.62 and 3.63.

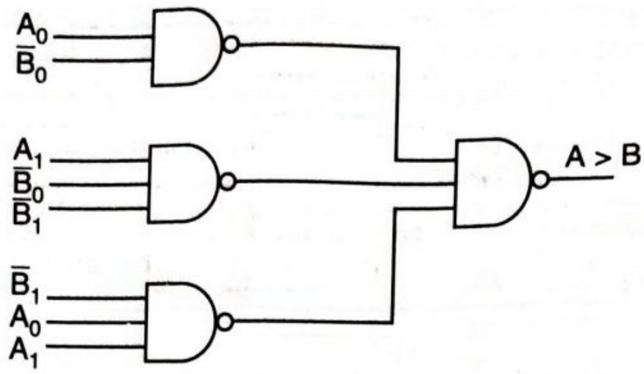

Fig. 3.61.

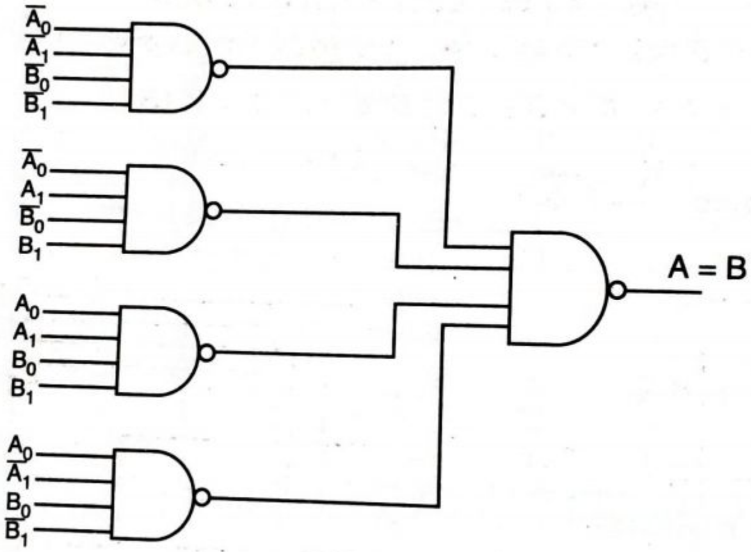

Fig. 3.62.

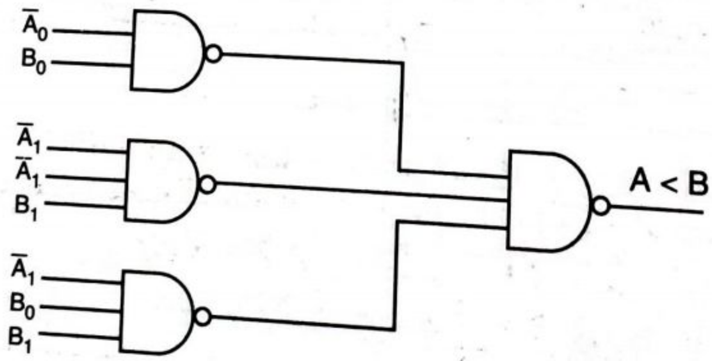

Fig. 3.63.

EXAMPLE 3.11. Implement the function $F(A, B, C) = \Sigma(1, 3, 5, 6)$ using decoder.

Solution: Since the function has 3-inputs variables, a 3 to 8 line decoder may be used. It is in the sum of the products of minterms m_1, m_3, m_5 and m_6 and so decoder output D_1, D_3, D_5 and D_6 may be OR gated to achieve the desired function. The designing is as follows :

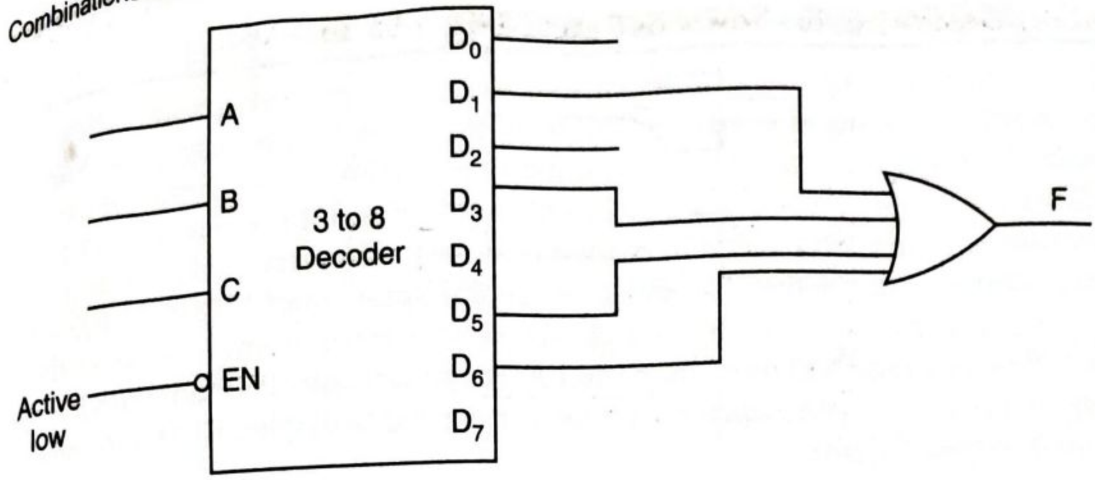

Fig. 3.64.

EXAMPLE 3.12. Design a full adder with decoder.

Solution: The output expression for sum and carry is given as :

001 + 010 + 100 + 111
1 2 4 7

$$S = \bar{X}\,\bar{A}B + \bar{X}A\bar{B} + X\bar{A}\,\bar{B} + XAB$$

$$C = \bar{X}AB + X\bar{A}B + XA\bar{B} + XAB$$

011 + 101 + 110 + 111
3 5 6 7

The designing is as follows :

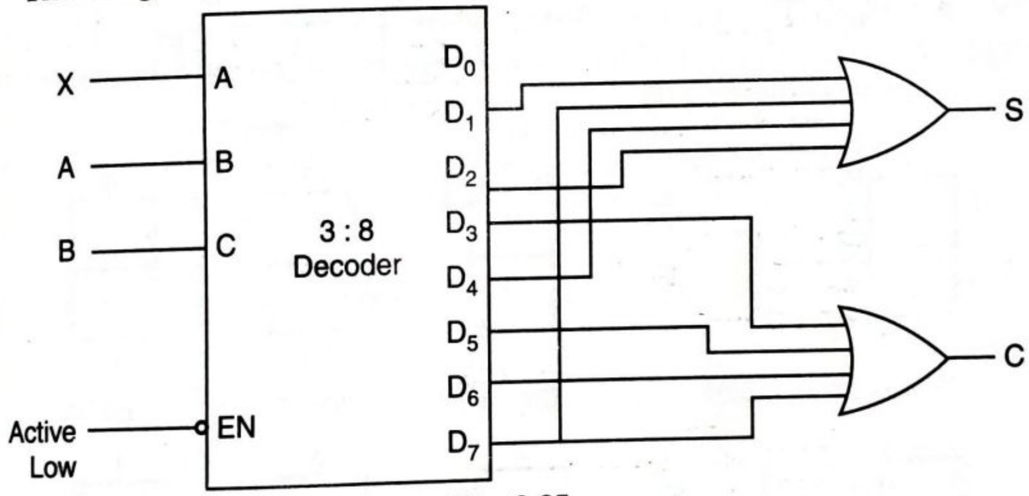

Fig. 3.65.

EXAMPLE 3.13. Design full subtractor using decoder.

Solution: The output expression for borrow and difference is as follows :

001 010 100 111
1 2 4 7

$$D = \bar{X}\,\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\,\bar{Z} + XYZ$$

$$B = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + \bar{X}YZ + XYZ$$

1-001
2-010
3-011
7-111

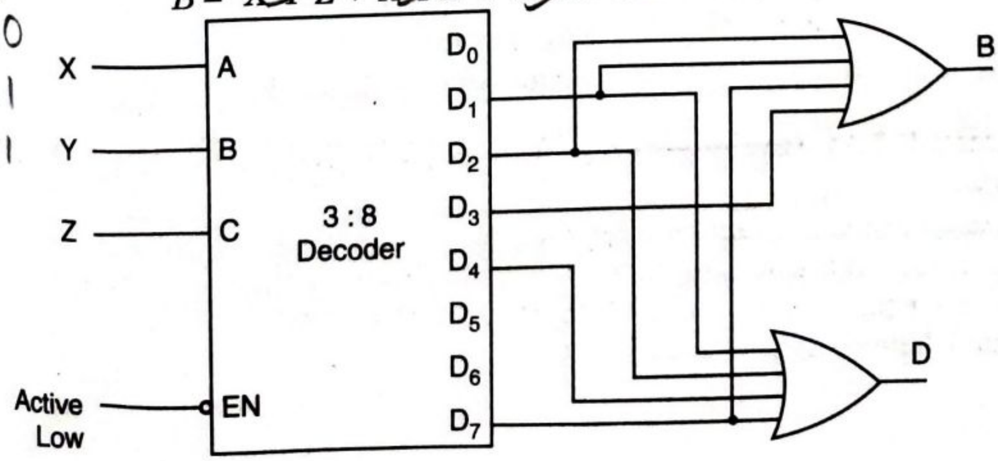

Fig. 3.66.